

## Product Overview

The NSi826x devices are high reliability six-channel digital isolators. The NSi826x device is safety certified by UL1577 support several insulation withstand voltage(3kV,3.75kV,5kV), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi826x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSi826x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi826x device supports to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

## Key Features

- Up to 5000V<sub>rms</sub> Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 200kV/us
- Chip level ESD: HBM: ±8kV
- High system level EMC performance:
  - Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -55°C~125°C
- RoHS-compliant packages:
  - SOP16(300mil)
  - SSOP16
  - SOP16(150mil)

## Safety Regulatory Approvals

- UL recognition: up to 5000V<sub>rms</sub> for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

## Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation

## Device Information

Part Number	Package	Body Size
NSi826x-DSWR	SOP16(300mil)	10.30mm × 7.50mm
NSi826x-DSSR	SSOP16	4.90mm × 3.90mm
NSi826x-DSPNR	SOP16(150mil)	9.90mm x 3.90mm

## Functional Block Diagrams

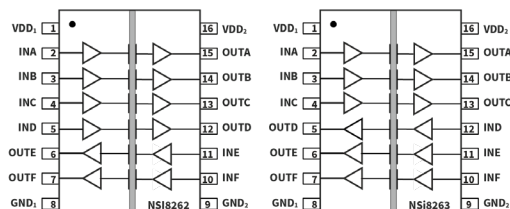
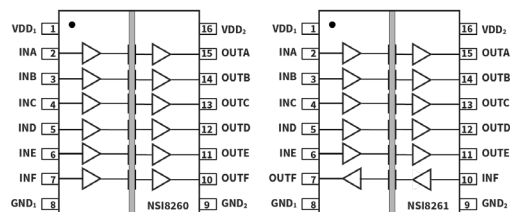


Figure 1. NSi826x Block Diagram

## INDEX

<b>1. PIN CONFIGURATION AND FUNCTIONS</b> .....	<b>3</b>
<b>2. ABSOLUTE MAXIMUM RATINGS</b> .....	<b>4</b>
<b>3. RECOMMENDED OPERATING CONDITIONS</b> .....	<b>6</b>
<b>4. THERMAL CHARACTERISTICS</b> .....	<b>6</b>
<b>5. SPECIFICATIONS</b> .....	<b>7</b>
5.1. ELECTRICAL CHARACTERISTICS.....	7
5.2. SUPPLY CURRENT CHARACTERISTICS – 5V SUPPLY.....	7
5.3. SUPPLY CURRENT CHARACTERISTICS –3.3V SUPPLY.....	9
5.4. SUPPLY CURRENT CHARACTERISTICS–2.5V SUPPLY.....	11
5.5. SWITCHING CHARACTERISTICS - 5V SUPPLY.....	12
5.6. SWITCHING CHARACTERISTICS - 3.3V SUPPLY.....	13
5.7. SWITCHING CHARACTERISTICS - 2.5V SUPPLY.....	13
5.8. TYPICAL PERFORMANCE CHARACTERISTICS.....	14
5.9. PARAMETER MEASUREMENT INFORMATION.....	15
<b>6. HIGH VOLTAGE FEATURE DESCRIPTION</b> .....	<b>16</b>
6.1. INSULATION AND SAFETY RELATED SPECIFICATIONS.....	16
6.2. SAFETY-LIMITING VALUES .....	17
6.3. REGULATORY INFORMATION.....	20
<b>7. FUNCTION DESCRIPTION</b> .....	<b>22</b>
7.1. OVERVIEW.....	22
7.2. OOK MODULATION .....	23
<b>8. APPLICATION NOTE</b> .....	<b>24</b>
8.1. TYPICAL APPLICATION CIRCUIT .....	24
8.2. PCB LAYOUT.....	24
8.3. HIGH SPEED PERFORMANCE.....	25
8.4. TYPICAL SUPPLY CURRENT EQUATIONS.....	25
<b>9. PACKAGE INFORMATION</b> .....	<b>26</b>
<b>10. ORDER INFORMATION</b> .....	<b>29</b>
<b>11. DOCUMENTATION SUPPORT</b> .....	<b>30</b>
<b>12. TAPE AND REEL INFORMATION</b> .....	<b>31</b>
<b>13. REVISION HISTORY</b> .....	<b>35</b>

# 1. Pin Configuration and Functions

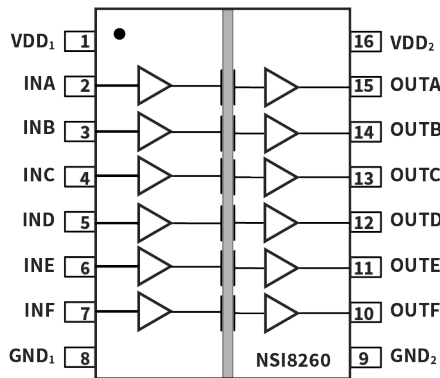


Figure 1.1 NSi8260 Package

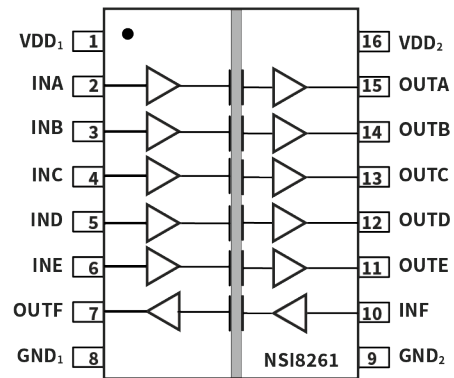


Figure 1.2 NSi8261 Package

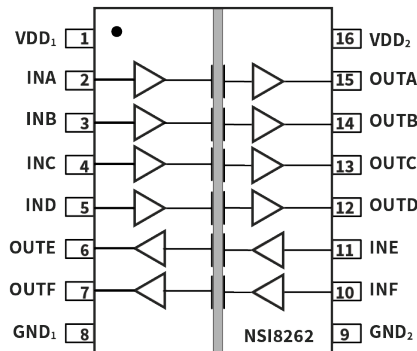


Figure 1.3 NSi8262 Package

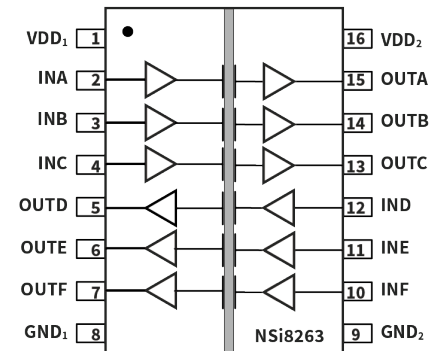


Figure 1.4 NSi8263 Package

Table 1.1 NSi8260/ NSi8261/ NSi8262 Pin Configuration and Description

<b>NSi8260 PIN NO.</b>	<b>NSi8261 PIN NO.</b>	<b>NSi8262 PIN NO.</b>	<b>NSi8263 PIN NO.</b>	<b>SYMBOL</b>	<b>FUNCTION</b>
1	1	1	1	VDD <sub>1</sub>	Power Supply for Isolator Side 1
2	2	2	2	INA	Logic Input A
3	3	3	3	INB	Logic Input B
4	4	4	4	INC	Logic Input C
5	5	5	12	IND	Logic Input D
6	6	11	11	INE	Logic Input E
7	10	10	10	INF	Logic Input F
8	8	8	8	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
9	9	9	9	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2

NSi8260 PIN NO.	NSi8261 PIN NO.	NSi8262 PIN NO.	NSi8263 PIN NO.	SYMBOL	FUNCTION
10	7	7	7	OUTF	Logic Output F
11	11	6	6	OUTE	Logic Output E
12	12	12	5	OUTD	Logic Output D
13	13	13	13	OUTC	Logic Output C
14	14	14	14	OUTB	Logic Output B
15	15	15	15	OUTA	Logic Output A
16	16	16	16	VDD2	Power Supply for Isolator Side 2

## 2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC, VIND, VINE, VIN F	-0.4		VDD+0.4	V	
Maximum Output Voltage	VOUTA, VOUTB, VOUTC, VOUTD, VOUTE, VOUTF	-0.4		VDD+0.4	V	
Maximum Input/Output Pulse Voltage	ALL I/O Pin	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V <sub>IOSM</sub>			6.25	kV	
Operating Temperature	T <sub>opr</sub>	-55		125	°C	
Junction Temperature	T <sub>j</sub>			150	°C	
Storage Temperature	T <sub>stg</sub>	-65		150	°C	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	



### 3. Recommended Operating Conditions

<i>Parameters</i>	<i>Symbol</i>	<i>min</i>	<i>typ</i>	<i>max</i>	<i>unit</i>
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	T <sub>opr</sub>	-55		125	°C
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			150	Mbps

### 4. Thermal Characteristics

<i>Parameters</i>	<i>Symbol</i>	<i>SOP16(300mil)</i>	<i>SSOP16</i>	<i>SOP16(150mil)</i>	<i>Unit</i>
IC Junction-to-Air Thermal Resistance	$\theta_{JA}$	60.3	86.5	78.9	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC (top)}$	24.0	26.9	41.1	°C/W
Junction-to-board thermal resistance	$\theta_{JB}$	29.3	36.6	49.5	°C/W

## 5. Specifications

### 5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD <sub>POR</sub>		2.2		V	POR threshold as during power-up
	VDD <sub>HYS</sub>		0.1		V	POR threshold Hysteresis
Input Threshold	V <sub>IT</sub>		1.6		V	Input Threshold at rising edge
	V <sub>IT_HYS</sub>		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V <sub>IH</sub>	2			V	
Low Level Input Voltage	V <sub>IL</sub>			0.8	V	
High Level Output Voltage	V <sub>OH</sub>	VDD-0.4			V	I <sub>OH</sub> = - 4mA
Low Level Output Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 4mA
Output Impedance	R <sub>out</sub>		50		ohm	
Input Pull high or low Current	I <sub>pull</sub>		8	15	µA	
Start Up Time after POR	t <sub>rs</sub>		10		µs	
Common Mode Transient Immunity	CMTI	±200	±250		kV/µs	See <a href="#">Figure 5.12</a> , C <sub>L</sub> = 15pF

### 5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSi8260</b>					
	I <sub>DD1</sub> (Q0)		1.39	3.09	mA	All Input 0V for NSi8260x0 Or All Input at supply for NSi8260x1
	I <sub>DD2</sub> (Q0)		3.41	5.63	mA	
	I <sub>DD1</sub> (Q1)		7.37	12.16	mA	All Input at supply for NSi8260x0 Or All Input 0V for NSi8260x1
	I <sub>DD2</sub> (Q1)		3.49	5.76	mA	
	I <sub>DD1</sub> (1M)		4.39	7.24	mA	All Input with 1Mbps,

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I <sub>DD2</sub> (1M)		3.67	6.06	mA	C <sub>L</sub> =15pF
	I <sub>DD1</sub> (10M)		4.71	7.77	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		5.66	9.34	mA	
	I <sub>DD1</sub> (100M)		7.47	14.94	mA	All Input with 100Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (100M)		23.8	55.22	mA	
<b>NSi8261</b>						
	I <sub>DD1</sub> (Q0)		1.73	2.85	mA	All Input 0V for NSi8261x0 Or All Input at supply for NSi8261x1
	I <sub>DD2</sub> (Q0)		3.07	5.07	mA	
	I <sub>DD1</sub> (Q1)		6.72	11.09	mA	All Input at supply for NSi8261x0 Or All Input 0V for NSi8261x1
	I <sub>DD2</sub> (Q1)		4.14	6.83	mA	
	I <sub>DD1</sub> (1M)		4.27	7.05	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.79	6.25	mA	
	I <sub>DD1</sub> (10M)		4.87	8.03	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		5.50	9.08	mA	
	I <sub>DD1</sub> (100M)		10.19	20.38	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		21.08	47.21	mA	
<b>NSi8262</b>						
	I <sub>DD1</sub> (Q0)		2.06	3.40	mA	All Input 0V for NSi8262x0 Or All Input at supply for NSi8262x1
	I <sub>DD2</sub> (Q0)		2.74	4.52	mA	
	I <sub>DD1</sub> (Q1)		6.08	10.03	mA	All Input at supply for NSi8262x0 Or All Input 0V for NSi8262x1
	I <sub>DD2</sub> (Q1)		4.78	7.89	mA	
	I <sub>DD1</sub> (1M)		4.15	6.85	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.91	6.45	mA	
	I <sub>DD1</sub> (10M)		5.03	8.29	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		5.34	8.82	mA	
	I <sub>DD1</sub> (100M)		12.91	25.83	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		18.36	39.2	mA	
<b>NSi8263</b>						
	I <sub>DD1</sub> (Q0)		2.40	3.96	mA	



Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I <sub>DD2</sub> (Q0)		2.40	3.96	mA	All Input 0V for NSi8263x0 Or All Input at supply for NSi8263x1
	I <sub>DD1</sub> (Q1)		5.43	8.96	mA	All Input at supply for NSi8263x0 Or All Input 0V for NSi8263x1
	I <sub>DD2</sub> (Q1)		5.43	8.96	mA	
	I <sub>DD1</sub> (1M)		4.03	6.65	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		4.03	6.65	mA	
	I <sub>DD1</sub> (10M)		5.19	8.56	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		5.19	8.56	mA	
	I <sub>DD1</sub> (100M)		15.64	31.27	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
I <sub>DD2</sub> (100M)		15.64	31.27	mA		

### 5.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSi8260</b>					
	I <sub>DD1</sub> (Q0)		1.33	3.00	mA	All Input 0V for NSi8260x0 Or All Input at supply for NSi8260x1
	I <sub>DD2</sub> (Q0)		3.36	5.54	mA	
	I <sub>DD1</sub> (Q1)		7.26	11.98	mA	All Input at supply for NSi8260x0 Or All Input 0V for NSi8260x1
	I <sub>DD2</sub> (Q1)		3.43	5.66	mA	
	I <sub>DD1</sub> (1M)		4.31	7.11	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.55	5.86	mA	
	I <sub>DD1</sub> (10M)		4.5	7.43	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.87	8.04	mA	
	I <sub>DD1</sub> (100M)		6.15	12.30	mA	All Input with 100Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (100M)		18.89	37.78	mA	
	<b>NSi8261</b>					
	I <sub>DD1</sub> (Q0)		1.67	2.75	mA	All Input 0V for NSi8261x0 Or All Input at supply for NSi8261x1
	I <sub>DD2</sub> (Q0)		3.02	4.99	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I <sub>DD1</sub> (Q1)		6.62	10.93	mA	All Input at supply for NSi8261x0 Or All Input 0V for NSi8261x1
	I <sub>DD2</sub> (Q1)		4.07	6.71	mA	
	I <sub>DD1</sub> (1M)		4.18	6.90	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.68	6.07	mA	
	I <sub>DD1</sub> (10M)		4.56	7.53	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.81	7.93	mA	
	I <sub>DD1</sub> (100M)		8.27	16.55	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		16.77	33.53	mA	
<b>NSi8262</b>						
	I <sub>DD1</sub> (Q0)		2.01	3.31	mA	All Input 0V for NSi8261x0 Or All Input at supply for NSi8261x1
	I <sub>DD2</sub> (Q0)		2.68	4.43	mA	
	I <sub>DD1</sub> (Q1)		5.98	9.87	mA	All Input at supply for NSi8261x0 Or All Input 0V for NSi8261x1
	I <sub>DD2</sub> (Q1)		4.71	7.77	mA	
	I <sub>DD1</sub> (1M)		4.06	6.69	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.80	6.28	mA	
	I <sub>DD1</sub> (10M)		4.62	7.63	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.75	7.83	mA	
	I <sub>DD1</sub> (100M)		10.40	20.79	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		14.64	29.29	mA	
<b>NSi8263</b>						
	I <sub>DD1</sub> (Q0)		2.35	3.87	mA	All Input 0V for NSi8262x0 Or All Input at supply for NSi8262x1
	I <sub>DD2</sub> (Q0)		2.35	3.87	mA	
	I <sub>DD1</sub> (Q1)		5.35	8.82	mA	All Input at supply for NSi8262x0 Or All Input 0V for NSi8262x1
	I <sub>DD2</sub> (Q1)		5.35	8.82	mA	
	I <sub>DD1</sub> (1M)		3.93	6.48	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.93	6.48	mA	
	I <sub>DD1</sub> (10M)		4.69	7.73	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.69	7.73	mA	
	I <sub>DD1</sub> (100M)		12.52	25.04	mA	All Input with 100Mbps,

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I <sub>DD2</sub> (100M)		12.52	25.04	mA	C <sub>L</sub> = 15pF

### 5.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSi8260</b>					
	I <sub>DD1</sub> (Q0)		1.29	2.94	mA	All Input 0V for NSi8260x0 Or All Input at supply for NSi8260x1
	I <sub>DD2</sub> (Q0)		3.33	5.49	mA	
	I <sub>DD1</sub> (Q1)		7	11.55	mA	All Input at supply for NSi8260x0 Or All Input 0V for NSi8260x1
	I <sub>DD2</sub> (Q1)		3.39	5.59	mA	
	I <sub>DD1</sub> (1M)		4.17	6.88	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.47	5.73	mA	
	I <sub>DD1</sub> (10M)		4.29	7.08	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.48	7.39	mA	
	I <sub>DD1</sub> (100M)		5.27	10.54	mA	All Input with 100Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (100M)		15.33	30.66	mA	
	<b>NSi8261</b>					
	I <sub>DD1</sub> (Q0)		1.63	2.69	mA	All Input 0V for NSi8261x0 Or All Input at supply for NSi8261x1
	I <sub>DD2</sub> (Q0)		2.99	4.93	mA	
	I <sub>DD1</sub> (Q1)		6.40	10.56	mA	All Input at supply for NSi8261x0 Or All Input 0V for NSi8261x1
	I <sub>DD2</sub> (Q1)		3.99	6.59	mA	
	I <sub>DD1</sub> (1M)		4.05	6.69	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.59	5.92	mA	
	I <sub>DD1</sub> (10M)		4.32	7.13	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.45	7.34	mA	
	I <sub>DD1</sub> (100M)		6.95	13.89	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		13.65	27.31	mA	
	<b>NSi8262</b>					

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I <sub>DD1</sub> (Q0)		1.97	3.25	mA	All Input 0V for NSi8261x0 Or All Input at supply for NSi8261x1
	I <sub>DD2</sub> (Q0)		2.65	4.37	mA	
	I <sub>DD1</sub> (Q1)		5.80	9.56	mA	All Input at supply for NSi8261x0 Or All Input 0V for NSi8261x1
	I <sub>DD2</sub> (Q1)		4.59	7.58	mA	
	I <sub>DD1</sub> (1M)		3.94	6.50	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.70	6.11	mA	
	I <sub>DD1</sub> (10M)		4.35	7.18	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.42	7.29	mA	
	I <sub>DD1</sub> (100M)		8.62	17.25	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		11.98	23.95	mA	
<b>NSi8263</b>						
	I <sub>DD1</sub> (Q0)		2.31	3.81	mA	All Input 0V for NSi8262x0 Or All Input at supply for NSi8262x1
	I <sub>DD2</sub> (Q0)		2.31	3.81	mA	
	I <sub>DD1</sub> (Q1)		5.20	8.57	mA	All Input at supply for NSi8262x0 Or All Input 0V for NSi8262x1
	I <sub>DD2</sub> (Q1)		5.20	8.57	mA	
	I <sub>DD1</sub> (1M)		3.82	6.30	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.82	6.30	mA	
	I <sub>DD1</sub> (10M)		4.39	7.24	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.39	7.24	mA	
	I <sub>DD1</sub> (100M)		10.30	20.60	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		10.30	20.60	mA	

### 5.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t <sub>PLH</sub>	2.5	6.54	15	ns	See <a href="#">Figure 5.11</a> , C <sub>L</sub> = 15pF

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	$t_{PHL}$	2.5	8.30	15	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Rising Time	$t_r$			5.0	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Falling Time	$t_f$			5.0	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT}(PK)$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	

### 5.6. Switching Characteristics - 3.3V Supply

( $VDD1=3.3V \pm 10\%$ ,  $VDD2=3.3V \pm 10\%$ ,  $T_a=-55^\circ C$  to  $125^\circ C$ . Unless otherwise noted, Typical values are at **VDD1 = 3.3V**, **VDD2 = 3.3V**,  $T_a = 25^\circ C$ )

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	$t_{PLH}$	2.5	7.5	15	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
	$t_{PHL}$	2.5	8.7	15	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Rising Time	$t_r$			5.0	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Falling Time	$t_f$			5.0	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT}(PK)$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	

### 5.7. Switching Characteristics - 2.5V Supply

( $VDD1=2.5V \pm 10\%$ ,  $VDD2=2.5V \pm 10\%$ ,  $T_a=-55^\circ C$  to  $125^\circ C$ . Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**,  $T_a = 25^\circ C$ )

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	$t_{PLH}$	2.5	9.0	15	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
	$t_{PHL}$	2.5	9.3	15	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Rising Time	$t_r$			5.0	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Falling Time	$t_f$			5.0	ns	See <a href="#">Figure 5.11</a> , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

### 5.8. Typical Performance Characteristics

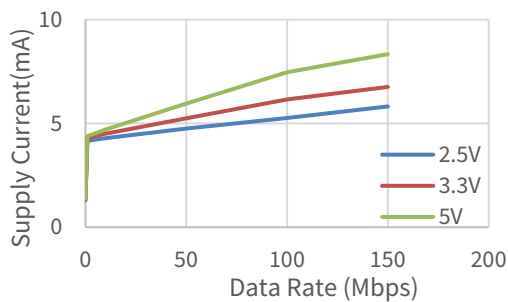


Figure 5.1 NSi8260 VDD1 Supply Current vs Data Rate

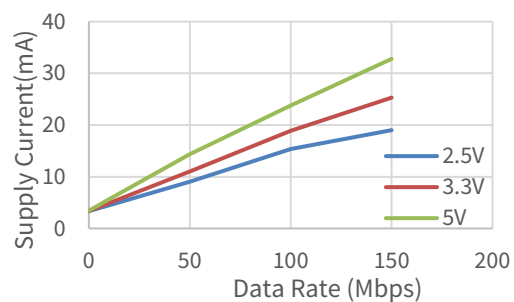


Figure 5.2 NSi8260 VDD2 Supply Current vs Data Rate

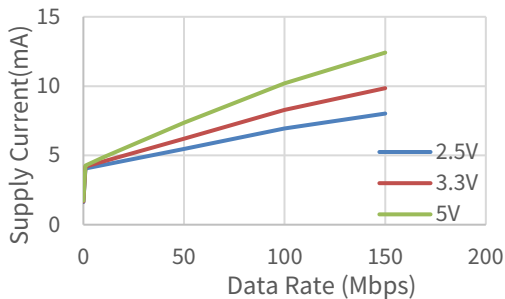


Figure 5.3 NSi8261 VDD1 Supply Current vs Data Rate

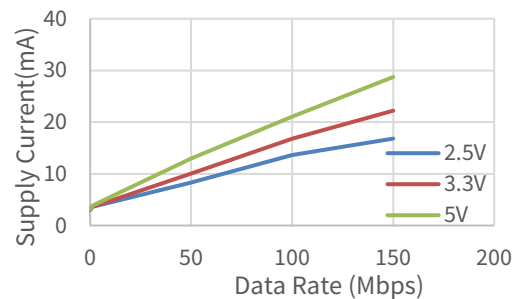


Figure 5.4 NSi8261 VDD2 Supply Current vs Data Rate

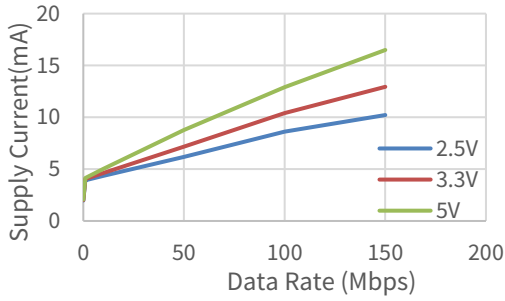


Figure 5.5 NSi8262 VDD1 Supply Current vs Data Rate

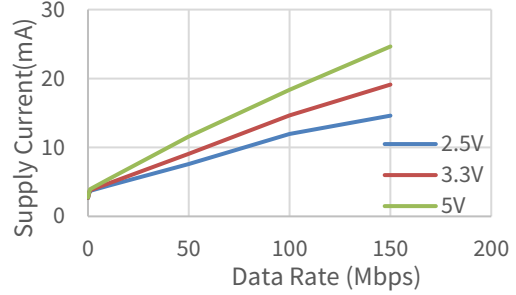


Figure 5.6 NSi8262 VDD2 Supply Current vs Data Rate

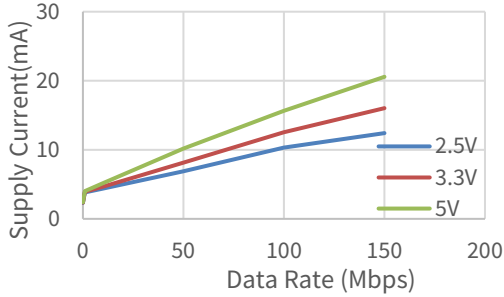


Figure 5.7 NSi8263 VDD1 Supply Current vs Data Rate

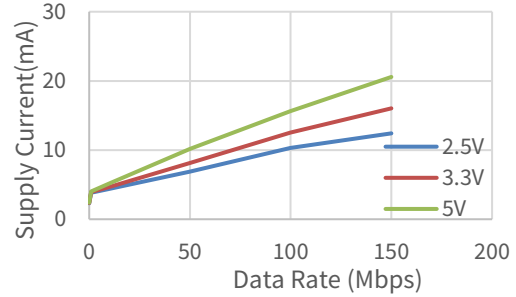


Figure 5.8 NSi8263 VDD2 Supply Current vs Data Rate

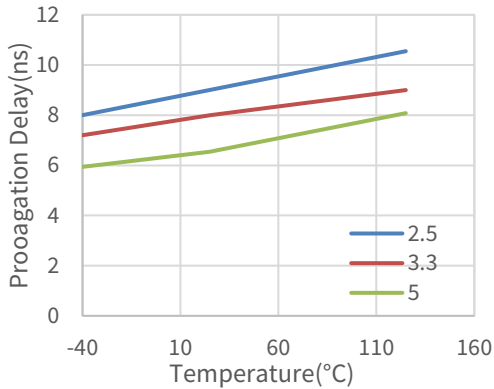


Figure 5.9 Rising Edge Propagation Delay Vs Temp

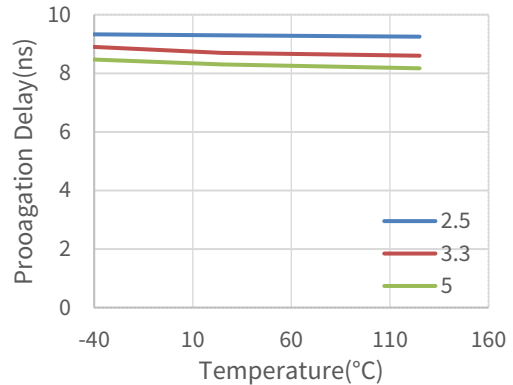


Figure 5.10 Falling Edge Propagation Delay Vs Temp

### 5.9. Parameter Measurement Information

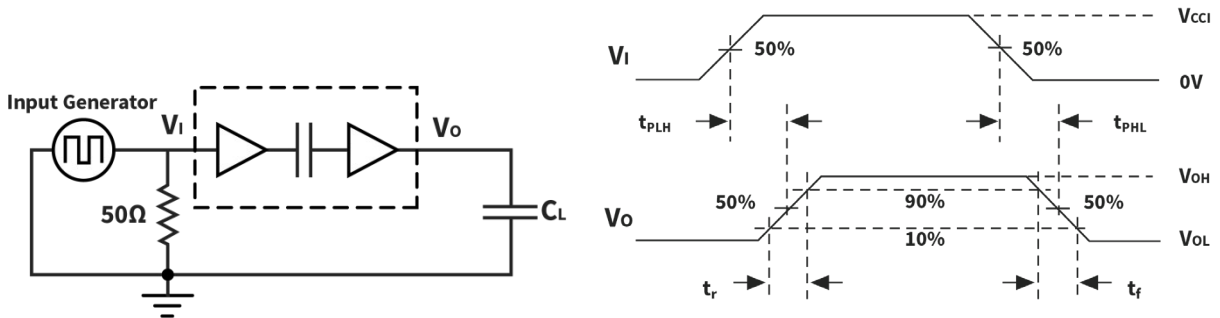


Figure 5.11 Switching Characteristics Test Circuit and Waveform

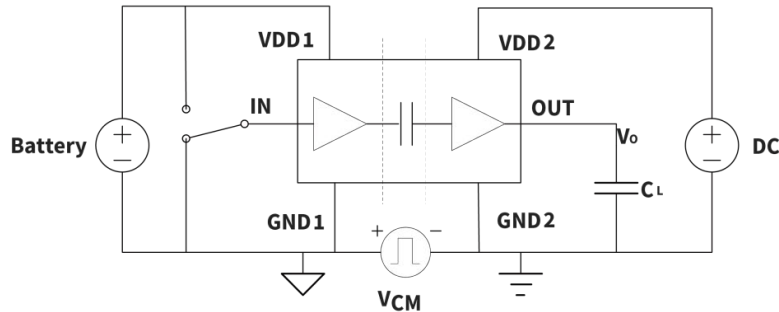


Figure 5.12 Common-Mode Transient Immunity Test Circuit

## 6. High Voltage Feature Description

### 6.1. Insulation and Safety Related Specifications

Description	Test Condition	Symbol	Value			Unit
			SSOP16	SOP16 (300mil)	SOP16 (150mil)	
Min. External Air Gap (Clearance)		CLR	3.9	8	4.0	mm
Min. External Tracking (Creepage)		CPG	3.9	8	4.0	mm
Distance through the Insulation		DTI	28			um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600			V
Material Group	IEC 60112		I			
Installation Classification per DIN VDE 0110						
For Rated Mains Voltage ≤ 150Vrms			I to III	I to IV	I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to II	I to IV	I to III	
For Rated Mains Voltage ≤ 600Vrms			I	I to IV	I to II	
For Rated Mains Voltage ≤ 1000Vrms			/	I to III	I to II	
Insulation Specification per DIN VDE V 0884-11:2017-01 <sup>1)</sup>						
Climatic Category			40/125/21			
Pollution Degree	per DIN VDE 0110, Table 1		2			
Maximum Working Isolation Voltage	AC voltage	V <sub>IOWM</sub>	400	1500	400	V <sub>RMS</sub>
	DC voltage		565	2121	565	V <sub>DC</sub>
Maximum Repetitive Isolation Voltage		V <sub>IORM</sub>	565	2121	565	V <sub>peak</sub>
Input to Output Test Voltage, Method B1	V <sub>ini. b</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = V <sub>IORM</sub> × 1.5, t <sub>ini</sub> = t <sub>m</sub> = 1 sec, q <sub>pd</sub> ≤ 5 pC,	V <sub>pd(m)</sub>	847	/	847	V <sub>peak</sub>



Description	Test Condition	Symbol	Value			Unit
	100% production test					
	$V_{ini. b} = V_{IOTM}$ , $V_{pd(m)} = V_{IORM} \times 1.875$ , $t_{ini} = t_m = 1 \text{ sec}$ , $q_{pd} \leq 5 \text{ pC}$ , 100% production test	$V_{pd(m)}$	/	3977	/	$V_{peak}$
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{ini. a} = V_{IOTM}$ , $V_{pd(m)} = V_{IORM} \times 1.3$ , $t_{ini} = 60 \text{ sec}$ , $t_m = 10 \text{ sec}$ , $q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	678	/	678	$V_{peak}$
	$V_{ini. a} = V_{IOTM}$ , $V_{pd(m)} = V_{IORM} \times 1.6$ , $t_{ini} = 60 \text{ sec}$ , $t_m = 10 \text{ sec}$ , $q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	/	3394	/	$V_{peak}$
Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{ini. a} = V_{IOTM}$ , $V_{pd(m)} = V_{IORM} \times 1.2$ , $t_{ini} = 60 \text{ sec}$ , $t_m = 10 \text{ sec}$ , $q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	678	2545	678	$V_{peak}$
Maximum Transient Isolation Voltage	$t = 60 \text{ sec}$	$V_{IOTM}$	5000	8000	6500	$V_{peak}$
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.3 \times V_{IOSM}$	$V_{IOSM}$	5384	/	5384	$V_{peak}$
	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$		/	6250	/	$V_{peak}$
Isolation Resistance	$V_{IO} = 500 \text{ V}$ , $T_{amb} = T_s$	$R_{IO}$	$>10^9$			$\Omega$
	$V_{IO} = 500 \text{ V}$ , $100 \text{ }^\circ\text{C} \leq T_{amb} \leq 125 \text{ }^\circ\text{C}$		$>10^{11}$			$\Omega$
Isolation Capacitance	$f = 1\text{MHz}$	$C_{IO}$	1.2			pF
Insulation Specification per UL1577						
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1 \text{ sec}$ , 100% production test	$V_{ISO}$	3000	5000	3750	$V_{rms}$

1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

## 6.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSi826x-DSWR

Description	Test Condition	Value	Unit
-------------	----------------	-------	------

Safety Supply Power	$R_{\theta JA} = 60.3 \text{ }^\circ\text{C/W}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$	2073	mW
Safety Supply Current	$R_{\theta JA} = 60.3 \text{ }^\circ\text{C/W}$ , $V_I = 5\text{V}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$	414	mA
Safety Temperature <sup>2)</sup>		150	$^\circ\text{C}$

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SOP16(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

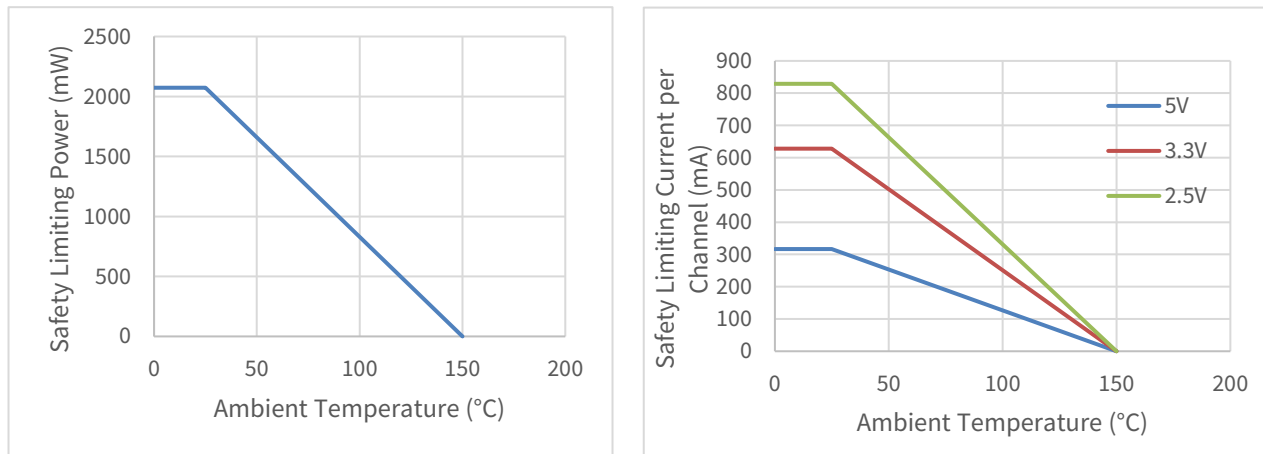


Figure 6.1 NSi826x-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi826x-DSSR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 86.5 \text{ }^\circ\text{C/W}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$	1445	mW
Safety Supply Current	$R_{\theta JA} = 86.5 \text{ }^\circ\text{C/W}$ , $V_I = 5\text{V}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$	289	mA
Safety Temperature <sup>2)</sup>		150	$^\circ\text{C}$

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SSOP16 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

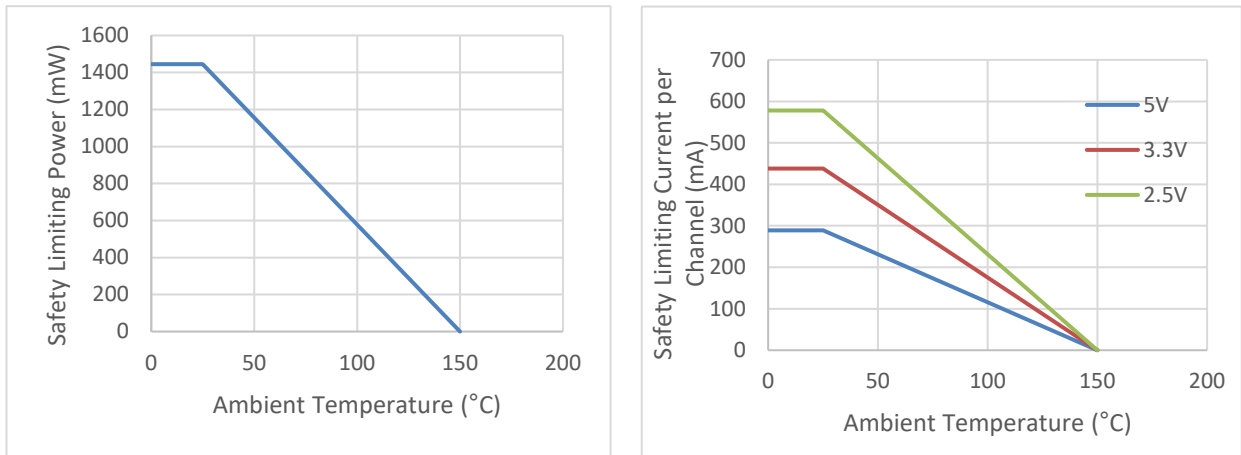


Figure 6.2 NSi826x-DSSR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi826x-DSPNR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 78.9^{\circ}\text{C}/\text{W}^{(1)}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$	1584	mW
Safety Supply Current	$R_{\theta JA} = 78.9^{\circ}\text{C}/\text{W}^{(1)}$ , $V_I = 5\text{V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$	316	mA
Safety Temperature <sup>2)</sup>		150	$^{\circ}\text{C}$

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SOP16(150mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

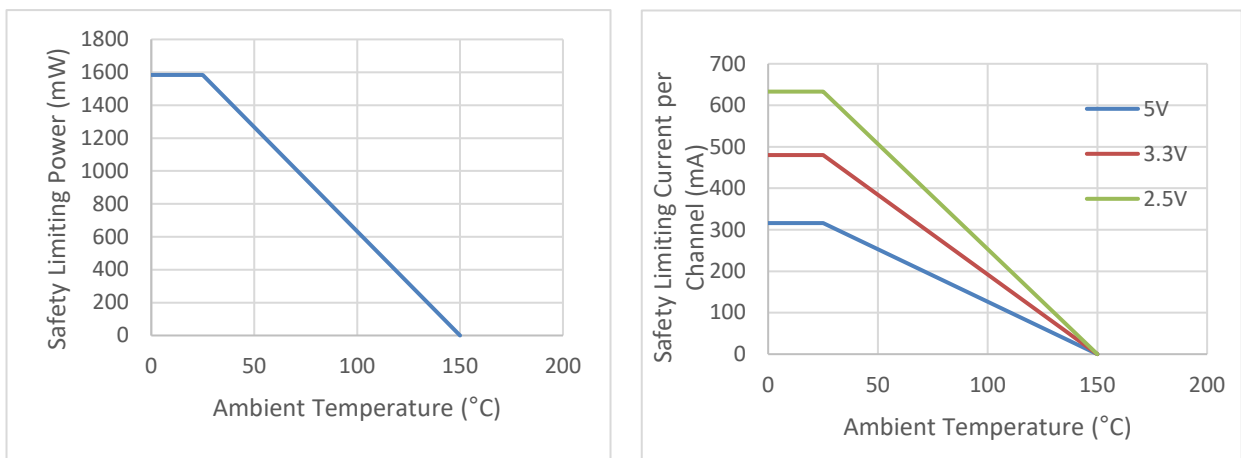


Figure 6.3 NSi826x-DSPNR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

### 6.3. Regulatory Information

The NSi826xW-DSWR are approved or pending approval by the organizations listed in table.

CUL	VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01
Certified by CQC11-471543-2012 GB4943.1-2011	Reinforce Insulation 2121Vpeak, $V_{IOSM}=6250\text{Vpeak}$	Reinforced insulation
File (UL-US-L500602-11-61808102-1)	File (UL-US-L500602-11-61808102-1)	File (5024579-4880-0002 / 276211)
		File (CQC20001264939)

The NSi826xS-DSSR are approved or pending approval by the organizations listed in table.

<b>CUL</b>		<b>VDE</b>	<b>CQC</b>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000V <sub>rms</sub> Isolation voltage	Single Protection, 3000V <sub>rms</sub> Isolation voltage	Basic Insulation 565V <sub>peak</sub> , VIOSM=5384V <sub>peak</sub>	Basic insulation
File (UL-US-L500602-11-61808102-1)	File (UL-US-L500602-11-61808102-1)	File (5024579-4880-0001 / 283544)	File (CQC19001233128)

The NSi826xN-DSPNR are approved or pending approval by the organizations listed in table.

<b>CUL</b>		<b>VDE</b>	<b>CQC</b>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750V <sub>rms</sub> Isolation voltage	Single Protection, 3750V <sub>rms</sub> Isolation voltage	Basic Insulation 565V <sub>peak</sub> , VIOSM=5384V <sub>peak</sub>	Basic insulation
File (pending)	File (pending)	File (pending)	File (pending)

## 7. Function Description

### 7.1. Overview

The NSi826x is a Six-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi826x devices are high reliability six-channel digital isolator. The NSi826x device is safety certified by UL1577 support 5kV<sub>rms</sub> insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi826x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSi826x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi826x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi826x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A after powering up.

Table 7.1 Output status vs. power status

<i>Input</i>	<i>VDD1 status</i>	<i>VDD2 status</i>	<i>Output</i>	<i>Comment</i>
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSi826xW0) H(NSi826xW1)	The output follows the same status with the input after input side VDD is powered on.
X	Ready	Unready	X	The output follows the same status with the input after output side VDD2 is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high VDD1 is input side power; VDD2 is out side power.				

### 7.2. OOK Modulation

NSi8266 is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 7.1 to Figure 7.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

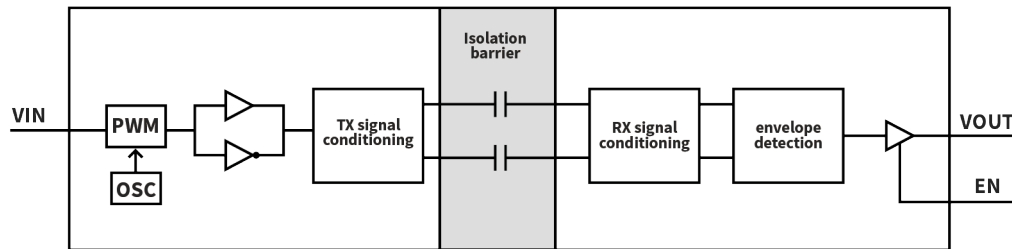


Figure 7.1 Single Channel Function Block Diagram

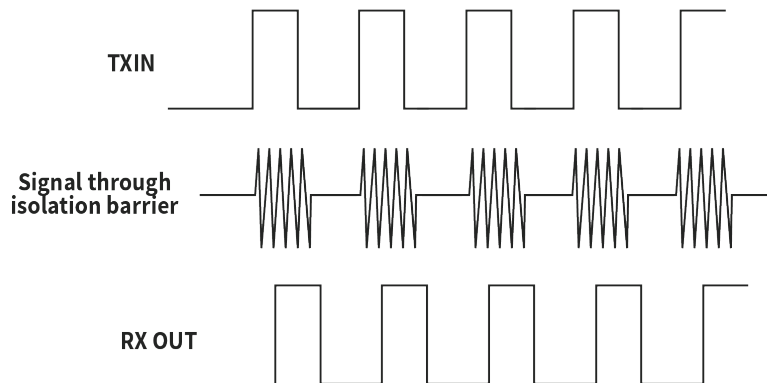


Figure 7.2 OOK Modulation

## 8. Application Note

### 8.1. Typical Application Circuit

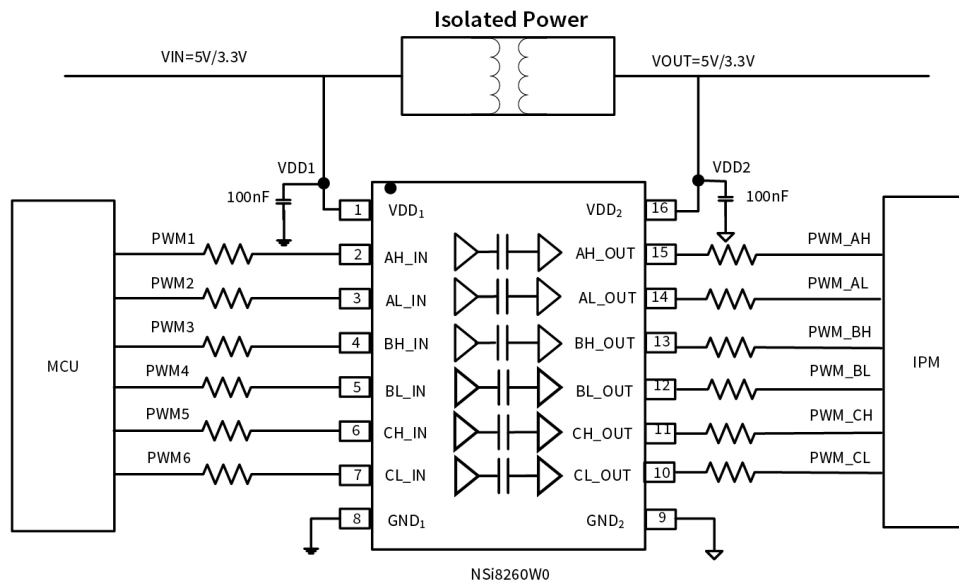


Figure 8.1 Typical PWM isolation circuit for IPM

### 8.2. PCB Layout

The NSi826x requires a 0.1  $\mu\text{F}$  bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300  $\Omega$ ) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50  $\Omega$ ,  $\pm 40\%$ . When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

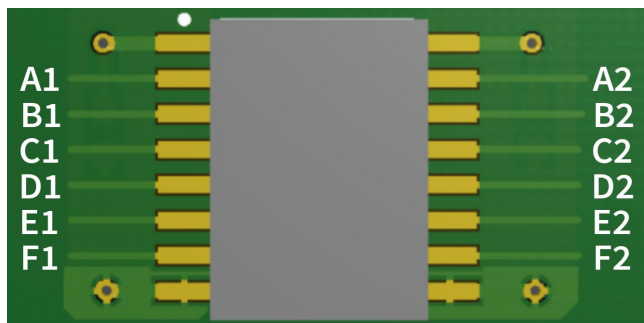


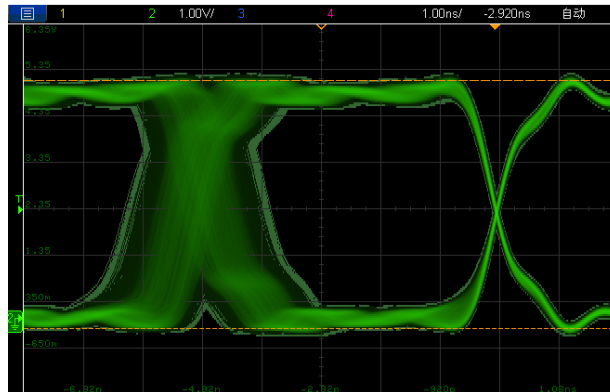
Figure 8.2 Recommended PCB Layout — Top Layer



Figure 8.3 Recommended PCB Layout — Bottom Layer



### 8.3. High Speed Performance



### 8.4. Typical Supply Current Equations

The typical supply current of NSi826x can be calculated using below equations.  $I_{DD1}$  and  $I_{DD2}$  are typical supply currents measured in mA,  $f$  is data rate measured in Mbps,  $C_L$  is the capacitive load measured in pF

#### NSi8260:

$$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$$

$$I_{DD2} = 1.36 + VDD2 * f * C_L * c1 * 10^{-9}$$

When  $a1$  is the channel number of default state input at side 1,  $b1$  is the channel number of non-default state input at side 1,  $c1$  is the channel number of switch signal input at side 1.

#### NSi8261:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$$

When  $b1$  is the channel number of non-default state input at side 1,  $c1$  is the channel number of switch signal input at side 1,  $b2$  is the channel number of non-default state input at side 2,  $c2$  is the channel number of switch signal input at side 2.

#### NSi8262:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$$

When  $b1$  is the channel number of non-default state input at side 1,  $c1$  is the channel number of switch signal input at side 1,  $b2$  is the channel number of non-default state input at side 2,  $c2$  is the channel number of switch signal input at side 2.

#### NSi8263:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$$

When  $b1$  is the channel number of non-default state input at side 1,  $c1$  is the channel number of switch signal input at side 1,  $b2$  is the channel number of non-default state input at side 2,  $c2$  is the channel number of switch signal input at side 2.

### 9. Package Information

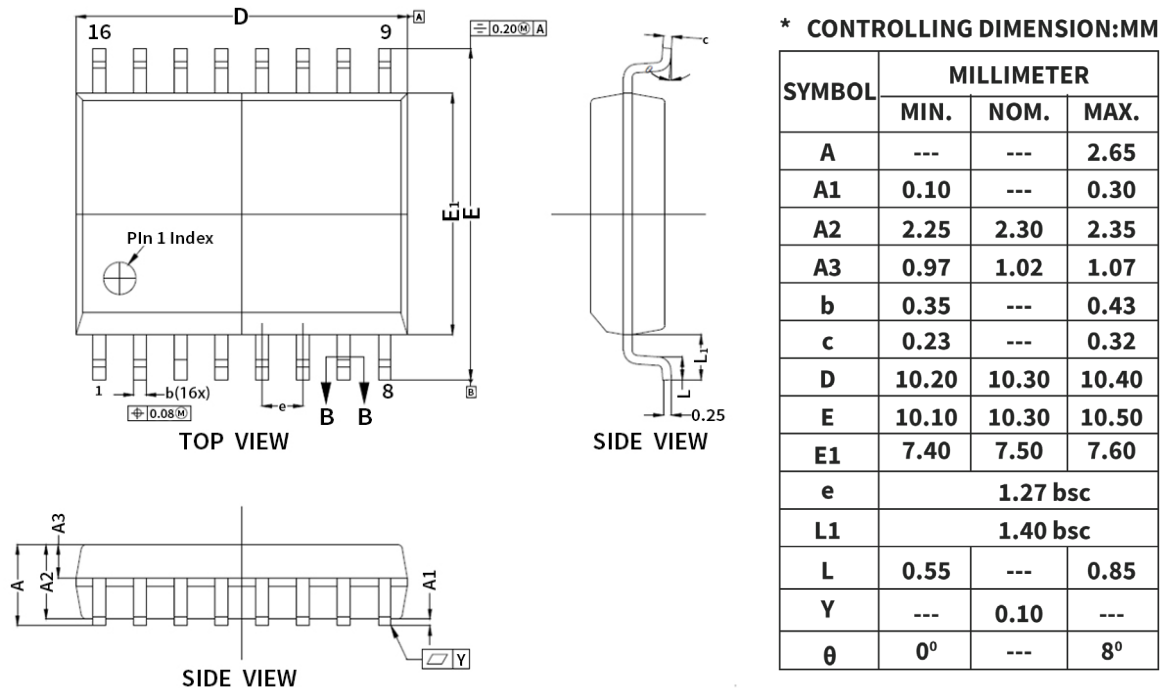
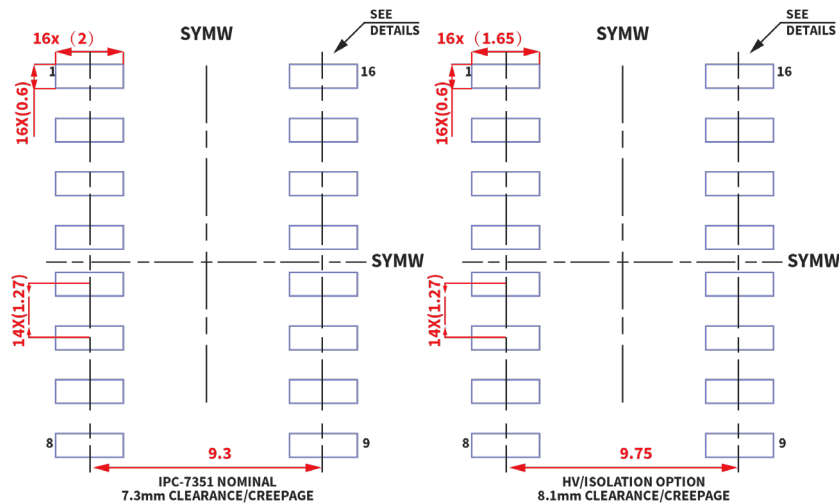


Figure 9.1 SOP16(300mil)/SOW16 Package Shape and Dimension in millimeters

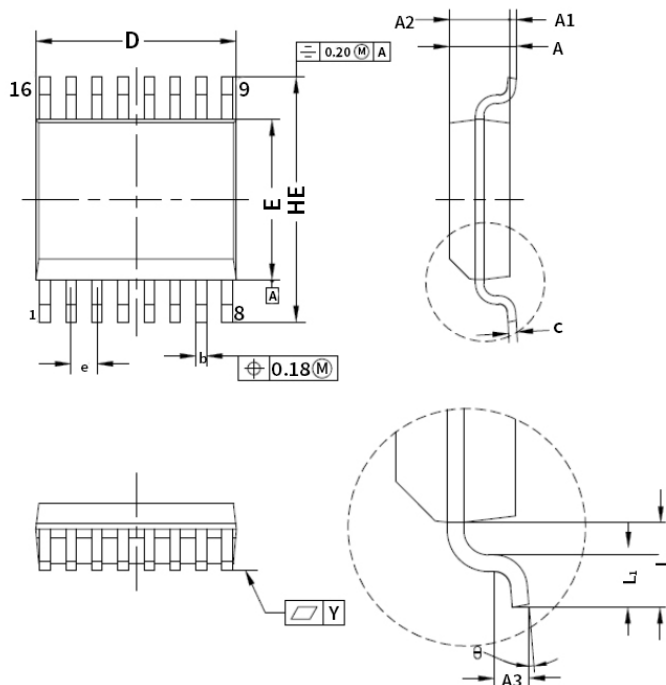


**LAND PATTERN EXAMPLE(mm)**



**SOLDER MASK DETAILS**

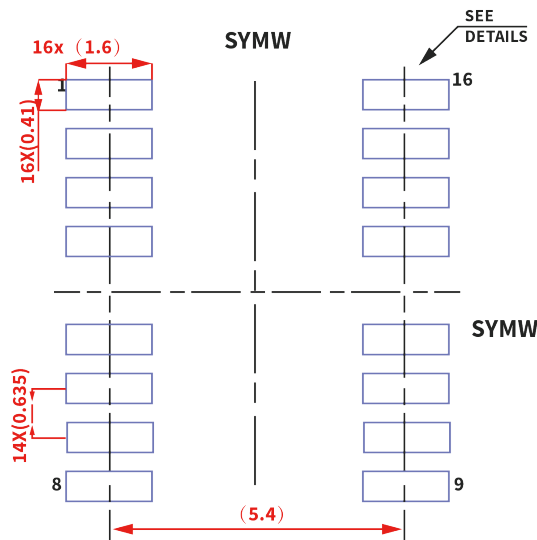
Figure 9.2 SOP16(300mil)/SOW16 Package Board Layout Example



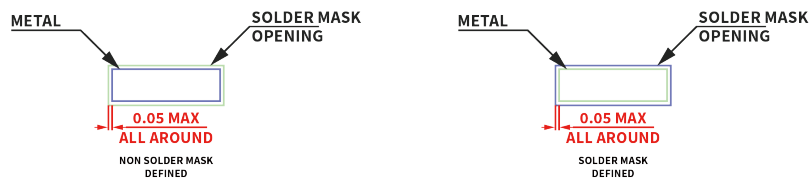
\* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.73	---	---	0.068
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.20	---	0.31	0.008	---	0.012
c	0.18	---	0.25	0.007	---	0.010
D	4.80	---	5.00	0.189	---	0.197
E	3.80	---	4.00	0.150	---	0.157
HE	5.80	---	6.20	0.228	---	0.244
e	0.635 bsc			0.025 bsc		
L	1.00 bsc			0.039 bsc		
L1	0.41	---	0.89	0.016	---	0.035
Y	---	0.09	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
θ	0°	---	8°	0°	---	8°

Figure 9.3 SSOP16 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 9.4 SSOP16 Package Board Layout Example

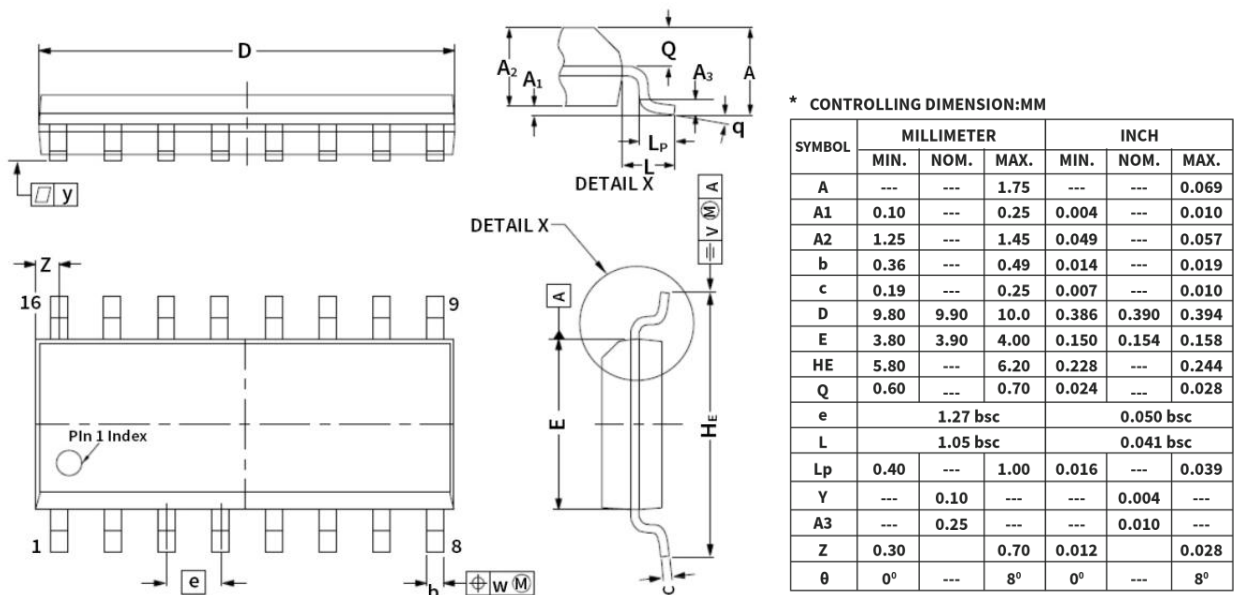
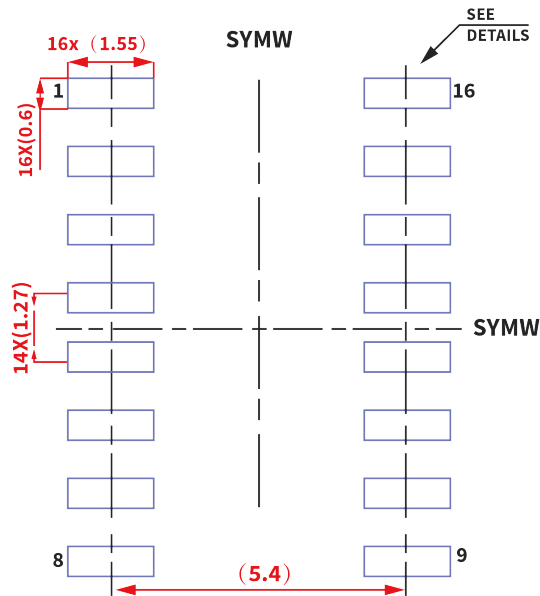
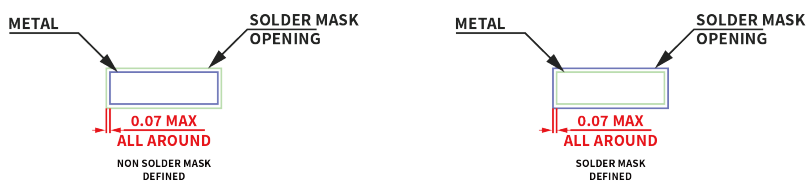


Figure 9.5 SOP16(150mil) Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

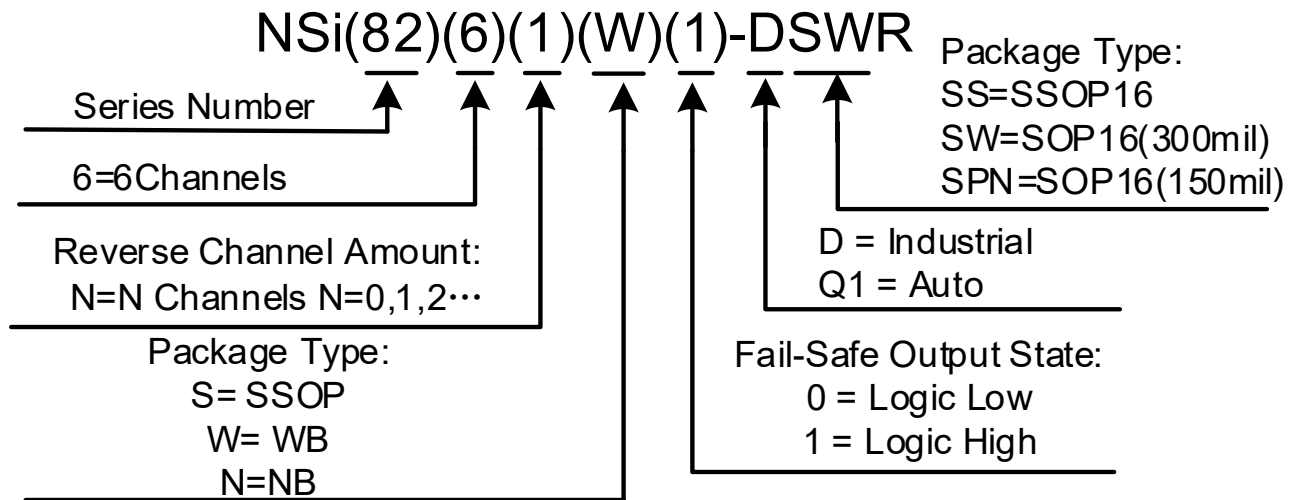
Figure 9.6 SOP16(150mil) Package Board Layout Example

### 10. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSi8260W 0-DSWR	5	6	0	150	Low	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSi8260W 1-DSWR	5	6	0	150	High	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSi8261W 0-DSWR	5	5	1	150	Low	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSi8261W 1-DSWR	5	5	1	150	High	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSi8262W 0-DSWR	5	4	2	150	Low	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSi8262W 1-DSWR	5	4	2	150	High	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSi8263W 0-DSWR	5	3	3	150	Low	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSi8263W 1-DSWR	5	3	3	150	High	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSi8260S 0-DSSR	3	6	0	150	Low	-55 to 125°C	1	SSOP16	SSOP16	2500
NSi8260S 1-DSSR	3	6	0	150	High	-55 to 125°C	1	SSOP16	SSOP16	2500
NSi8261S 0-DSSR	3	5	1	150	Low	-55 to 125°C	1	SSOP16	SSOP16	2500
NSi8261S 1-DSSR	3	5	1	150	High	-55 to 125°C	1	SSOP16	SSOP16	2500
NSi8262S 0-DSSR	3	4	2	150	Low	-55 to 125°C	1	SSOP16	SSOP16	2500
NSi8262S 1-DSSR	3	4	2	150	High	-55 to 125°C	1	SSOP16	SSOP16	2500
NSi8263S 0-DSSR	3	3	3	150	Low	-55 to 125°C	1	SSOP16	SSOP16	2500
NSi8263S 1-DSSR	3	3	3	150	High	-55 to 125°C	1	SSOP16	SSOP16	2500
NSi8260N 0-DSPNR	3	6	0	150	Low	-55 to 125°C	1	SOP16 (150mil)	SOP16	2500
NSi8260N 1-DSPNR	3	6	0	150	High	-55 to 125°C	1	SOP16 (150mil)	SOP16	2500
NSi8261N 0-DSPNR	3	5	1	150	Low	-55 to 125°C	1	SOP16 (150mil)	SOP16	2500
NSi8261N 1-DSPNR	3	5	1	150	High	-55 to 125°C	1	SOP16 (150mil)	SOP16	2500
NSi8262N 0-DSPNR	3	4	2	150	Low	-55 to 125°C	1	SOP16 (150mil)	SOP16	2500
NSi8262N 1-DSPNR	3	4	2	150	High	-55 to 125°C	1	SOP16 (150mil)	SOP16	2500
NSi8263N 0-DSPNR	3	3	3	150	Low	-55 to 125°C	1	SOP16 (150mil)	SOP16	2500
NSi8263N 1-DSPNR	3	3	3	150	High	-55 to 125°C	1	SOP16 (150mil)	SOP16	2500

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

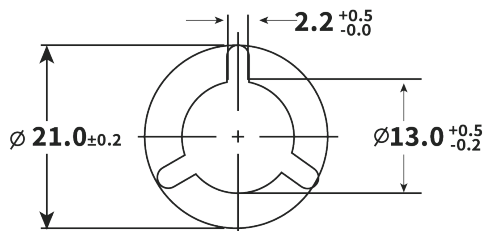
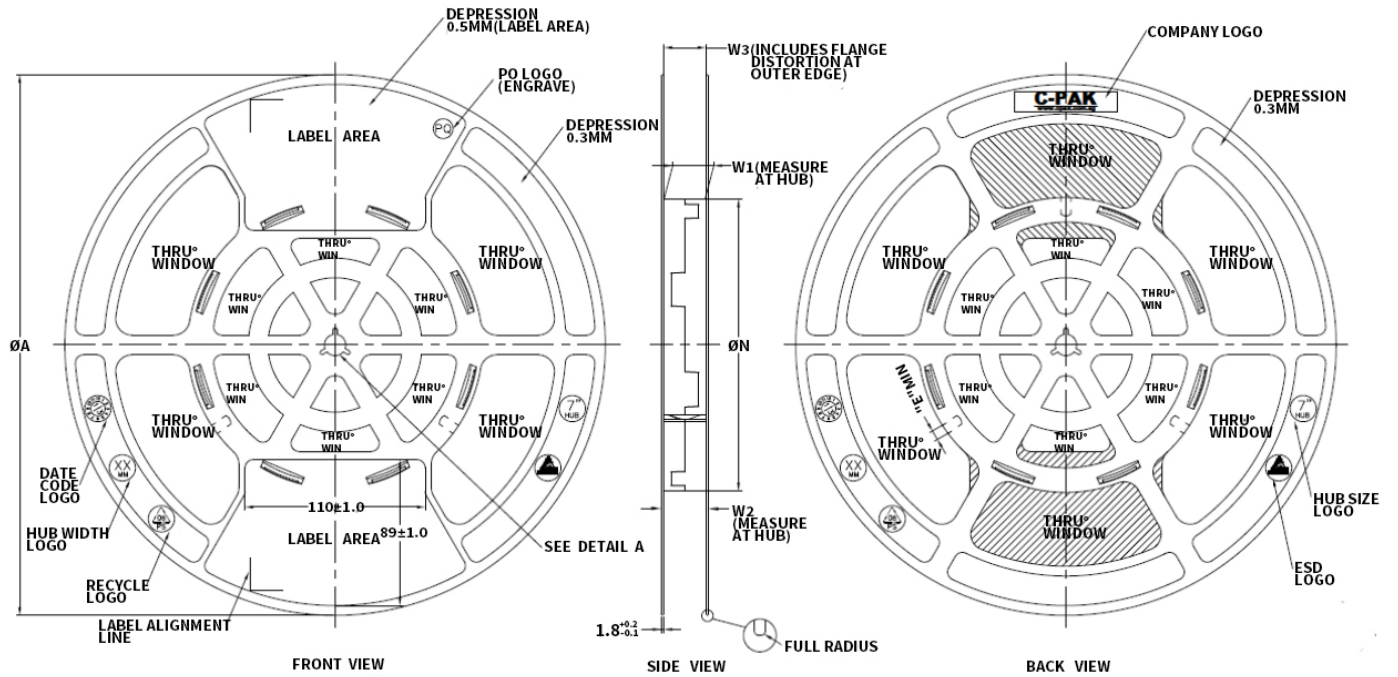
**Part Number Rule:**



**11. Documentation Support**

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>	<i>Isolator selection guide</i>
NSi826x	tbd	tbd	tbd	tbd

### 12. Tape and Reel Information

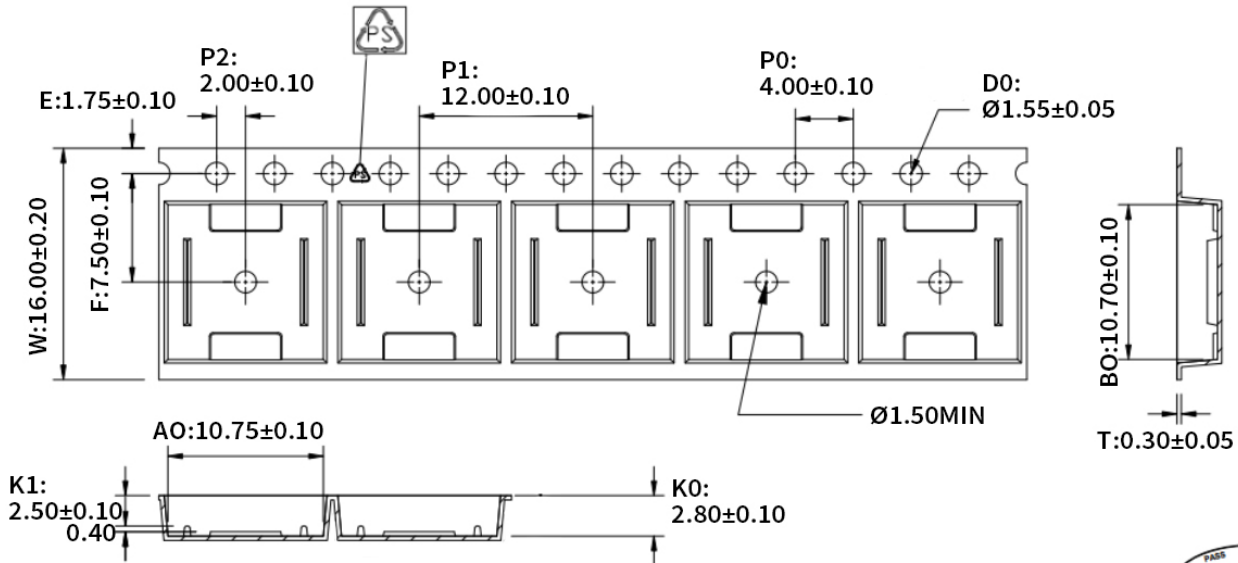


**ARBOR HOLE  
DETAIL A  
SCALE: 3:1**

PRODUCT SPECIFICATION						
TAPE WIDTH	$\varnothing A \pm 2.0$	$\varnothing N \pm 2.0$	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW $10^{12}$	ANTISTATIC	ALL TYPES
B	$10^6$ TO $10^{11}$	STATIC DISSIPATIVE	BLACK ONLY
C	$10^5$ & BELOW $10^5$	CONDUCTIVE(GENERIC)	BLACK ONLY
E	$10^9$ TO $10^{11}$	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)



1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness:  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122 )
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:  $10^5 \sim 10^{10} \Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

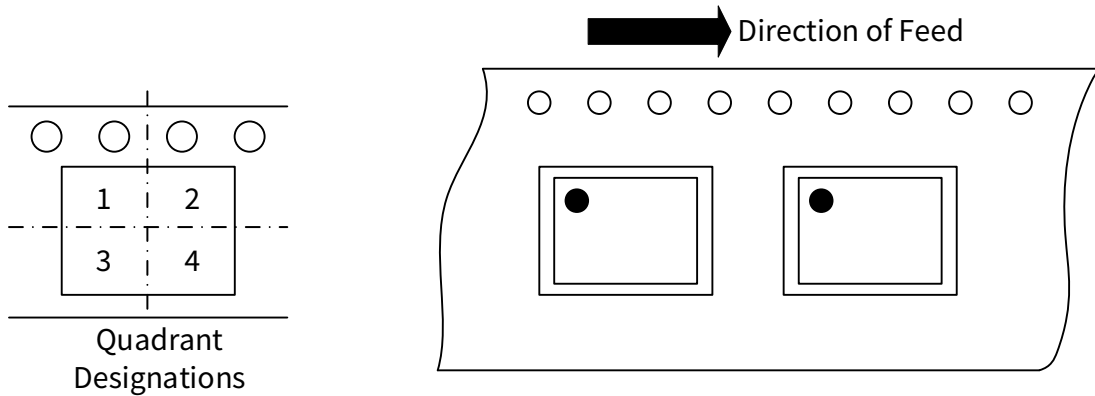


Figure 12.2 Tape Information of SOP16(300mil)



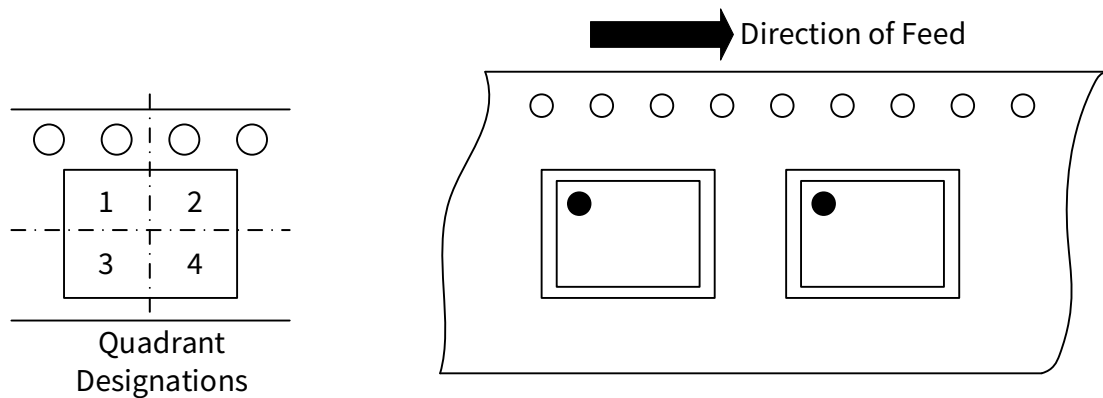
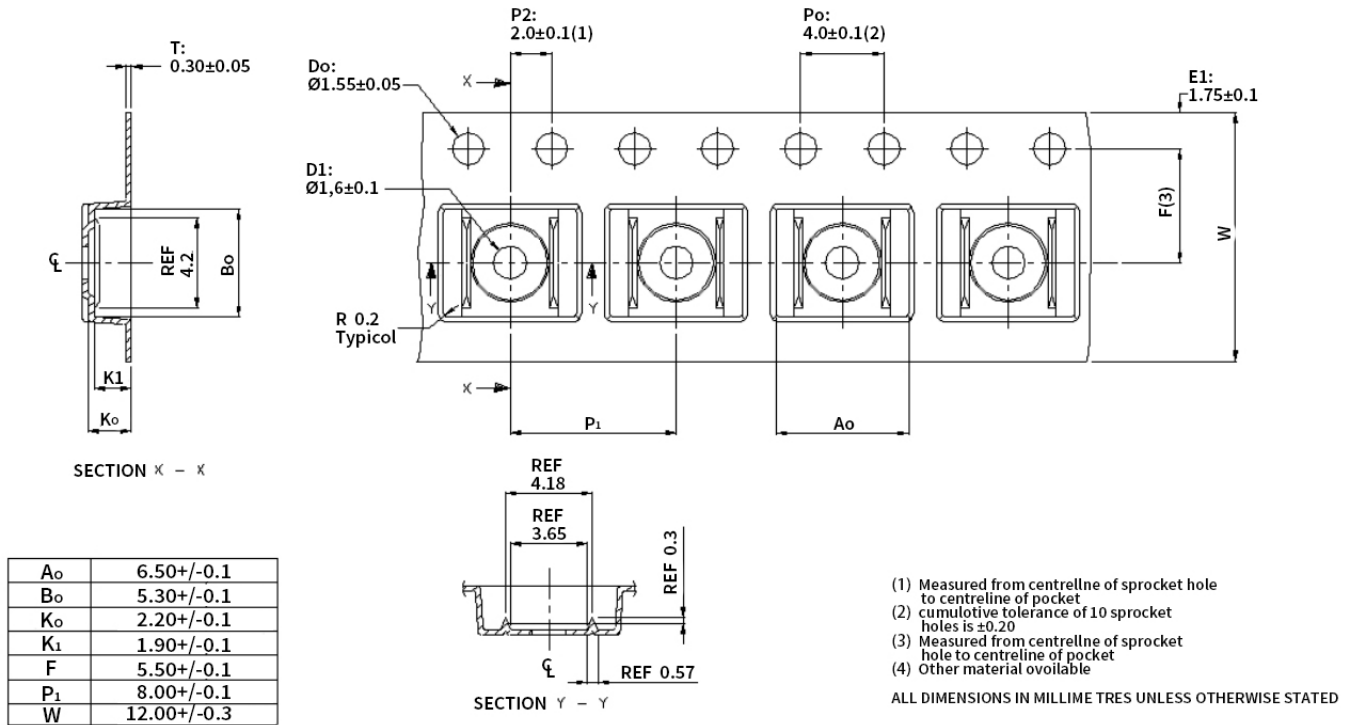


Figure 12.3 Tape Information of SSOP16

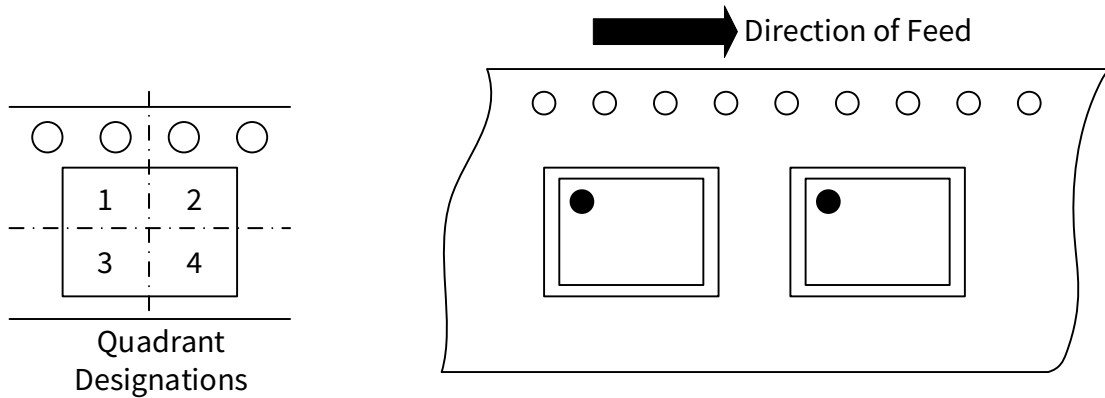
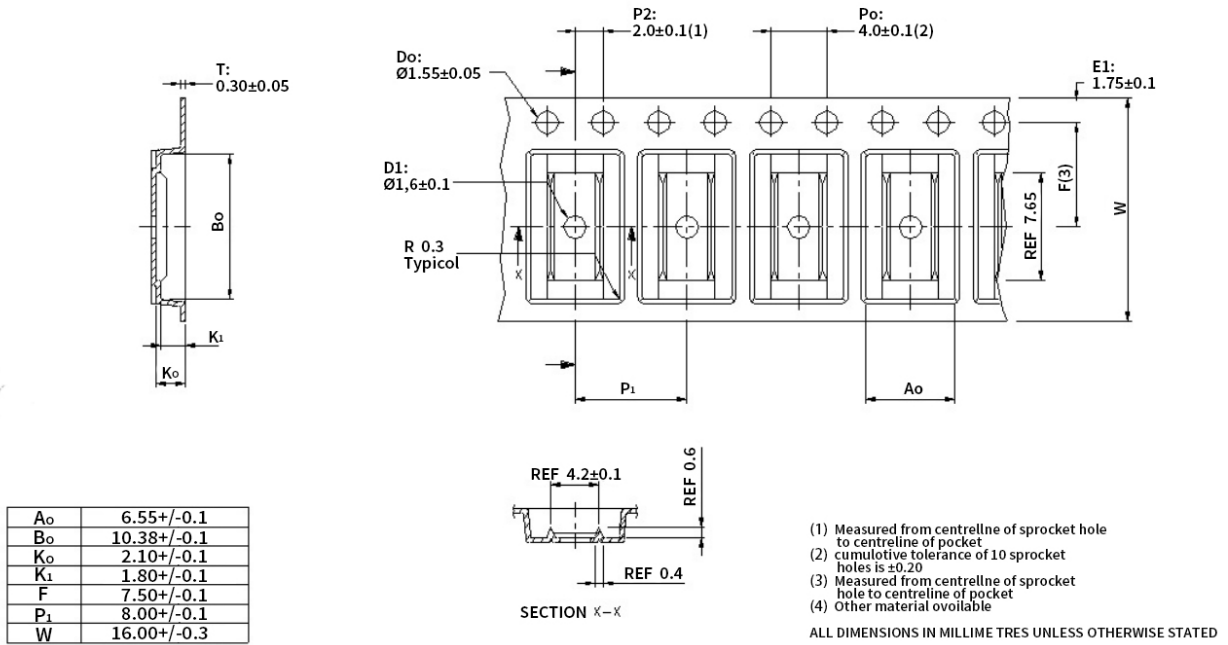


Figure 12.4 Tape Information of SOP16(150mil)

### 13. Revision history

<b>Revision</b>	<b>Description</b>	<b>Date</b>
1.0	Initial version	2020/11/13
1.1	Changed tape and reel information	2020/12/20
1.2	Updated Safety Regulatory	2021/6/28
1.3	Updated Safety-Limiting Values. Update SSOP16 Package Shape and Dimension in millimeters. Changed AEC-Q100 description.	2022/4/25
1.4	Update SOW16\SSOP16 Package Board Layout Example	2022/6/6
1.5	Update SSOP16 CTI and VDE file.	2023/1/12
1.6	Update SOP16 Package, Typical Supply Current Equations	2023/3/22

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