Low-power dual digital isolators

1 Features

- Qualified for automotive applications
- AEC-Q100 Qualified with the following results:
  - Device temperature grade 1: -40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level H3A
  - Device CDM ESD classification level C4
- Propagation delay less than 20 ns
- Low power consumption
- Safety and regulatory approvals
  - 4242 V_{PK} Isolation per VDE, 2.5 kVrms isolation per UL 1577, CSA approved per IEC 60950-1 and IEC 61010-1 End Equipment Standards
- 50 kV/µs Transient immunity typical
- Operates from 3.3 V or 5 V Supply and logic levels

2 Applications

- Opto-coupler replacement in:
  - Servo control interface
  - Motor control
  - Power supply
  - Battery packs

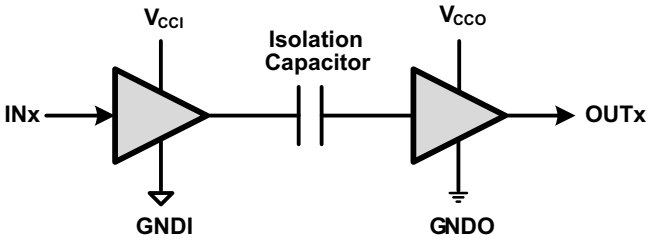
3 Description

The ISO7421E-Q1 provides double galvanic isolation of up to 2.5 KVrms for 1 minute per UL. This digital isolator has two isolation channels in a bi-directional configuration. Each isolation channel has a logic input and output buffer separated by a silicon oxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

The devices have TTL input thresholds and require two supply voltages, 3.3 V or 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply.

Note: The ISO7421E-Q1 is specified for signaling rates up to 50 Mbps. Due to their fast response time, under most cases, these devices will also transmit data with much shorter pulse widths. Designers should add external filtering to remove spurious signals with input pulse duration < 20 ns if desired.

Simplified Schematic

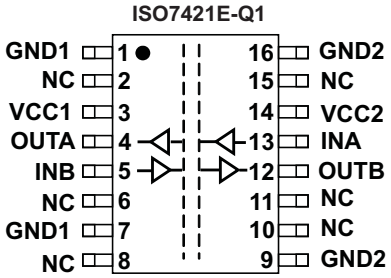


(1) V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

(2) V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

4 Pin Configuration and Functions

16-Pin SSOP
Top View



NC = No Internal Connection

Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	ISO7421E-Q1		
INA	13	I	Input, channel A
INB	5	–	Input, channel B
GND1	1, 7	–	Ground connection for V_{CC1}
GND2	9, 16	O	Ground connection for V_{CC2}
OUTA	4	O	Output, channel A
OUTB	12	–	Output, channel B
V_{CC1}	14	–	Power supply, V_{CC1}
V_{CC2}	14	-	Power supply, V_{CC2}
NC	2, 6, 8, 10, 11, 15		No Connect Pin

4.1 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

4.1 Device Function Table

INPUT SIDE V_{CC} (V_{CCI})(1)	OUTPUT SIDE V_{CC} (V_{CCO})(1)	INPUT (IN)(1)	OUTPUT (OUT)(1)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered Up (V_{CC} ≥ 3.15V); PD = Powered Down (V_{CC} ≤ 2.4V); X = Irrelevant; H = High Level; L = Low Level

4.2 Available Options

PRODUCT	RATED T_A	MARKED AS	ORDERING NUMBER
ISO7421E-Q1	–40°C to 125°C	ISO7421EQ	ISO7421EQDWRQ1

5 Absolute Maximum Ratings(1)

					VALUE		UNIT
					MIN	MAX	
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5	6	V
V_I	Voltage at IN, OUT				–0.5	V_{CC} + 0.5(3)	V
I_O	Output Current					±15	mA
ESD	Electrostatic discharge	Human Body Model	AEC-Q100 Classification Level H3A	All pins		4	kV
		Charged Device Model	AEC-Q100 Classification Level C4			1	kV
T_J	Maximum junction temperature					150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings(1) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V. A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.

6 Thermal Information

THERMAL METRIC(1)		ISO7421E-Q1 DW (16 Pins)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	79.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.6	
θ_{JB}	Junction-to-board thermal resistance	51.2	
ψ_{JT}	Junction-to-top characterization parameter	18.0	
ψ_{JB}	Junction-to-board characterization parameter	42.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	
P_D	Device power dissipation, Vcc1 = Vcc2 = 5.25 V, T_J = 150°C, C_L = 15 pF, Input a 0.5 MHz 50% duty cycle square wave	42	mW

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage - 3.3V Operation	3.15	3.3	3.45	V
	Supply voltage - 5V Operation	4.75	5	5.25	
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level output voltage	2		V_{CC}	V
V_{IL}	Low-level output voltage	0		0.8	V
T_A	Ambient Temperature	-40		125	°C
T_J (1)	Junction temperature	–40		136	°C
$1/t_{ui}$	Signaling rate	0		50	Mbps
t_{ui}	Input pulse duration	1			µs

(1) To maintain the recommended operating conditions for T_J, see the *Package Thermal Characteristics* table and the *Icc Equations* section of this data sheet

8 Electrical Characteristics

V_{CC1} and V_{CC2} at 5 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 1		V_{CC} –0.8	4.6		V
		I_{OH} = –20 µA; See Figure 1		V_{CC} –0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See Figure 3		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		2.3	3.6	mA
I_{CC2}			AC Input: C_L = 15 pF		2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15 pF		2.9	4.5	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			6	9.1	
I_{CC2}					6	9.1	

9 Switching Characteristics

V_{CC1} and V_{CC2} at 5 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		9	14	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.3	3.7	ns
$t_{sk(pp)}$	Part-to-part skew time				4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.6	ns
t_r	Output signal rise time	See Figure 1		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		µs

(1) Also known as pulse skew.

10 Electrical Characteristics

V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 1	5-V side	V_{CC} –0.8	4.6		V
			3.3-V side	V_{CC} –0.4	3		
		I_{OH} = –20 µA; See Figure 1		V_{CC} –0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See Figure 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		2.3	3.6	mA
I_{CC2}			AC Input: C_L = 15 pF		1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15 pF		2.9	4.5	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			6	9.1	
I_{CC2}					3.8	5.8	

11 Switching Characteristics

V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		10	17	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5.6	ns
$t_{sk(pp)}$	Part-to-part skew time				6.3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		µs

(1) Also known as pulse skew.

12 Electrical Characteristics

V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 1	5-V side	V_{CC} –0.8	4.6		V
			3.3-V side	V_{CC} –0.4	3		
		I_{OH} = –20 µA; See Figure 1		V_{CC} –0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See Figure 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		1.8	2.8	mA
I_{CC2}			AC Input: C_L = 15 pF		2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15 pF		2.2	3.2	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			3.8	5.8	
I_{CC2}					6	9.1	

13 Switching Characteristics

V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		10	17	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time				8.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		µs

(1) Also known as pulse skew.

14 Electrical Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 1		V_{CC} –0.4	3		V
		I_{OH} = –20 µA; See Figure 1		V_{CC} –0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}					µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See Figure 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		1.8	2.8	mA
I_{CC2}			AC Input: C_L = 15 pF		1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15 pF		2.2	3.2	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			3.8	5.8	
I_{CC2}					3.8	5.8	

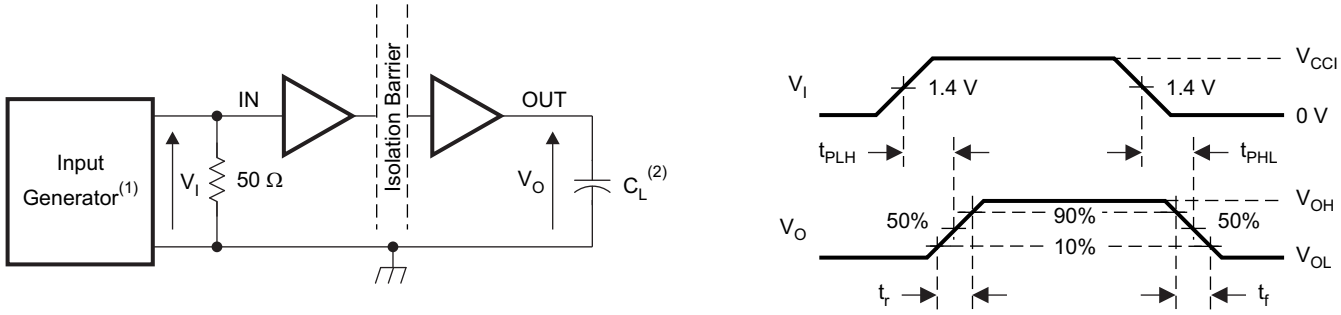
15 Switching Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		12	20	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			1	5	ns
$t_{sk(pp)}$	Part-to-part skew time				6.8	ns
$t_{sk(o)}$	Channel-to-channel output skew time				5.5	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		µs

(1) Also known as pulse skew.

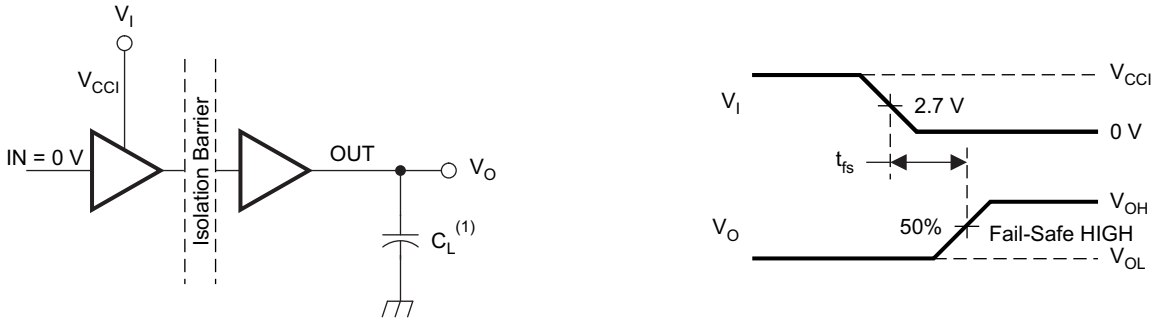
16 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

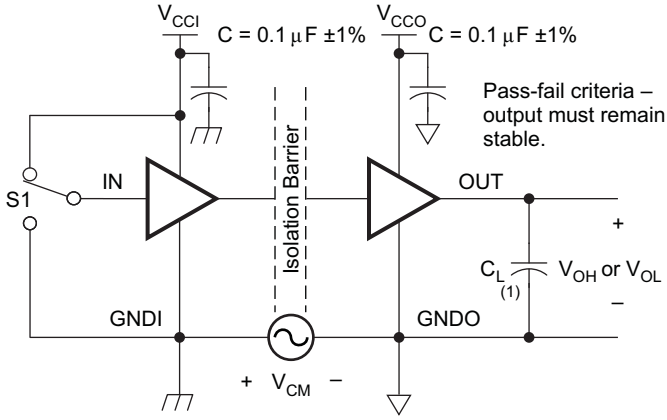
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

17 Device Information

17.1 Package Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	7.6			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	7.6			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN EN 60112 (VDE 0303-11)	≥400			V
	Minimum internal gap (Internal Clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance input to output(1)	V_{IO} = 0.4 sin(2πft), f = 1 MHz		2		pF
C_I	Input capacitance to ground(2)	$V_I = V_{CC}/2$ + 0.4 sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

17.2 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation Classification	Rated mains voltages <= 150 Vrms	I - IV
	Rated mains voltages <= 300 Vrms	I - IV
	Rated mains voltages <= 400 Vrms	I - III

17.3 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		1414	Vpeak
V_{PR}	Input to output test voltage	Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial discharge < 5 pC	2262	Vpeak
		After Input/Output Safety Test Subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC	1697	
		Method b1, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	2651	
V_{IOTM}	Transient overvoltage	t = 60 sec (qualification)	4242	Vpeak
V_{ISO}	Isolation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 sec (qualification)	2500	Vrms
		V_{TEST} = 1.2 x V_{ISO}, t = 1 sec (100% production)	3000	
R_S	Insulation resistance	V_{TEST} = 500 V at T_S = 150°C	$>10^9$	Ω
	Pollution degree		2	

17.4 Regulatory Information

VDE	CSA	UL
Certified according to DIN VDE V 0884-11:2017-01	Approved according to IEC 60950-1 and IEC 61010-1	Recognized under UL 1577 Component Recognition Program
Certificate Number: 40047657	Master Contract Number: 220991	File Number: E181974

17.5 IEC Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Is	Safety input, output, or supply current	θ_{JA} =212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			112	mA
		θ_{JA} =212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			171	
Ts	Maximum Case Temperature				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

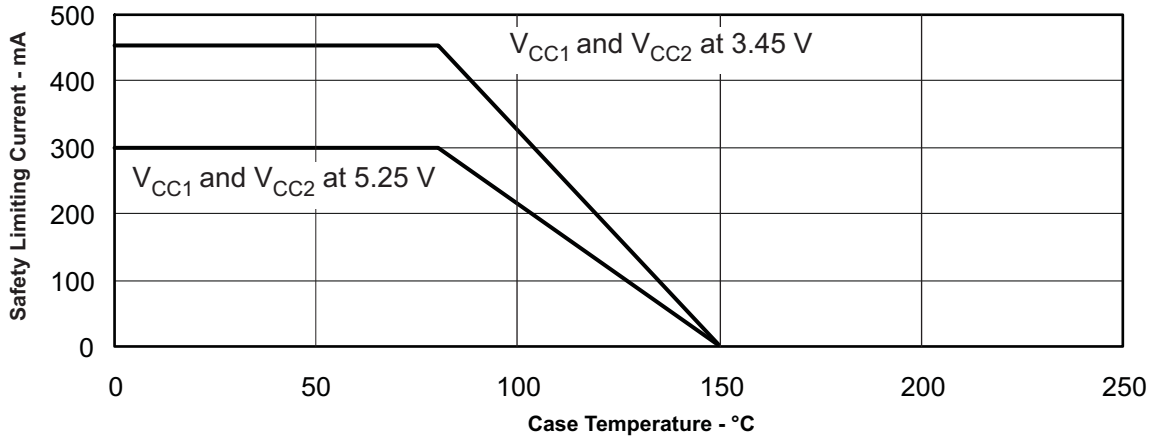


Figure 4. DW-16 Theta-JC Thermal Derating Curve per IEC 60747-5-2

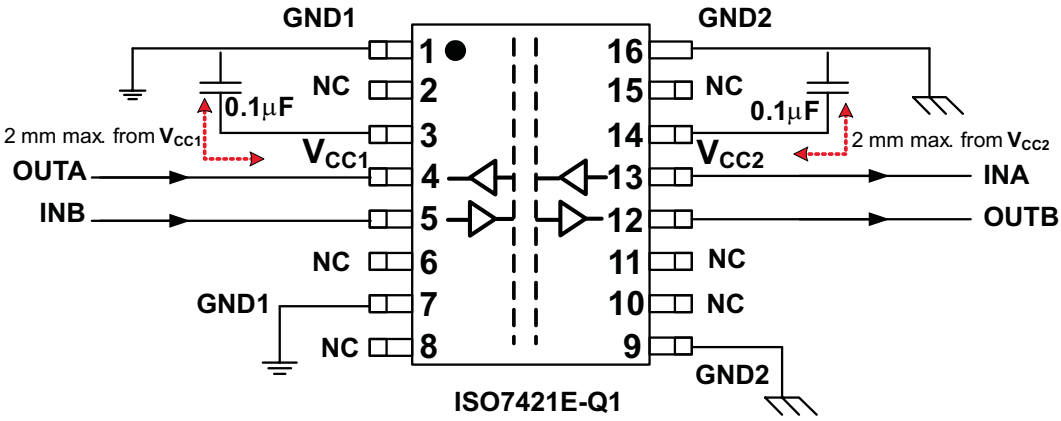


Figure 5. Typical ISO7421E-Q1 Application Circuit

17.6 Equivalent Input And Output Schematic Diagrams

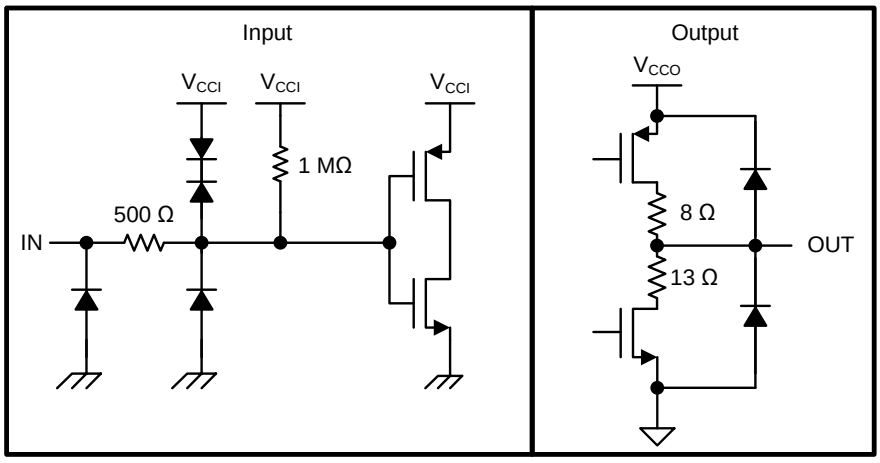


Figure 6. I/O Schematic

18 Typical Characteristics

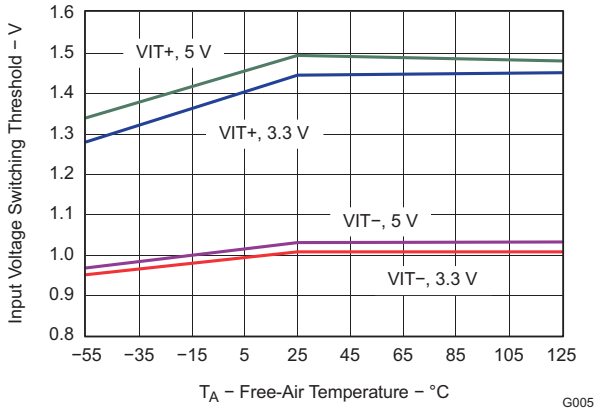


Figure 7. Input Voltage Switching Threshold Vs Free-air Temperature

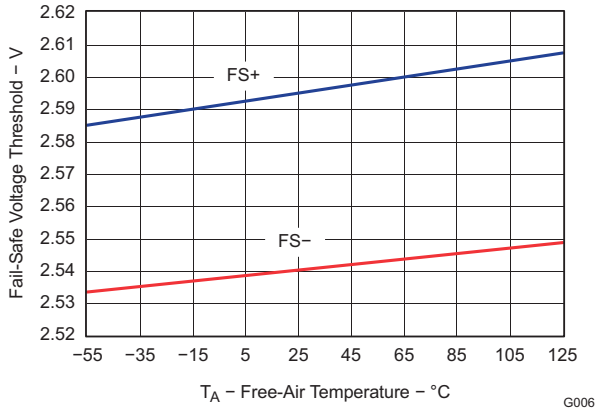


Figure 8. Fail-safe Voltage Threshold Vs Free-air Temperature

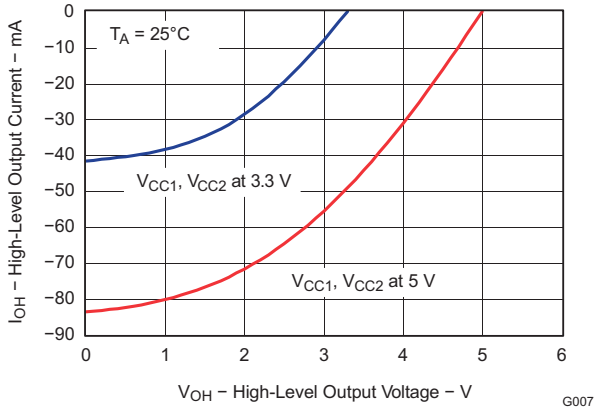


Figure 9. High-level Output Current Vs High-level Output Voltage

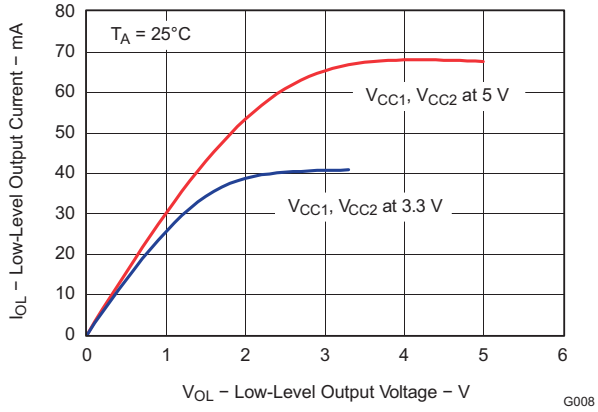


Figure 10. Low-level Output Current Vs Low-level Output Voltage

19 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2012) to Revision C **Page**

- Deleted FEATURES bullet "Wide Ambient Temperature: –40°C to 125°C" since it was a duplicate entry. 1
- Changed FEATURES bullet From: "4 kV peak Maximum Isolation, 2.5 kVrms per UL 1577, IEC/VDE and CSA Approved, IEC 60950-1, IEC 61010-1 End Equipment Standards Approved. All Approvals Pending." To: "4242 V_{PK} Isolation per VDE, 2.5 kVrms Isolation per UL 1577, CSA Approved per IEC 60950-1 and IEC 61010-1 End Equipment Standards" 1
- Changed From:"The ISO7421E-Q1 provides double galvanic isolation..." To:"The ISO7421E-Q1 provides galvanic isolation..." in Description section. 1
- Added Simplified Schematic of the device 1
- Changed column titles From:"INPUT SIDE (VCC)" To:"INPUT SIDE V_{CC} (V_{CCI})" and From:"OUTPUT SIDE (VCC)" To:"OUTPUT SIDE V_{CC} (V_{CCO})" in Device Function Table 3
- Changed MAX VALUE for V_I From: "6 V" To: "V_{CC} + 0.5 V" 3
- Added : "Maximum voltage must not exceed 6 V. A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output." 3
- Deleted Supply Current parameters with V_{CC1} and V_{CC2} at 5 V ± 5% for ISO7420x in Electrical Characteristics table since ISO7420x is not included in the data sheet. 5
- Deleted Supply Current parameters with V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5% for ISO7420x in Electrical Characteristics table since ISO7420x is not included in the data sheet. 6
- Deleted Supply Current parameters with V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5% for ISO7420x in Electrical Characteristics table since ISO7420x is not included in the data sheet. 7
- Deleted Supply Current parameters with V_{CC1} and V_{CC2} at 3.3 V ± 5% for ISO7420x in Electrical Characteristics table since ISO7420x is not included in the data sheet. 8
- Changed V_{CC1} to V_{CCI} and Vcc/2 to 50% in Figure 1 9
- Changed Vcc1 to V_{CCI} and IN From:"0V or V_{CC1}" To:"0 V" in Figure 2 9
- Corrected 'Ground' symbols on both sides of the Isolation Barrier in Figure 3 9
- Changed MIN specification for Clearance or L(I01) From: "8.34 mm" To:"7.6 mm" in Package Characteristics table. 10
- Changed MIN specification for Creepage or L(I02) From: "8.1 mm" To:"7.6 mm" in Package Characteristics table. 10
- Changed CTI TEST CONDITIONS From: " DIN IEC 60112 / VDE 0303 Part 1" To: "DIN EN 60112 (VDE 0303-11)" 10
- Added "V_{TEST} = 1.2 x V_{ISO}" to V_{ISO} parameter TEST CONDITIONS in Insulation Characteristics table 11
- Changed VDE standard name From: "IEC 60747-5-2" To:"DIN VDE V 0884-11:2017-01" and document reference From:"File Number: Pending" To:"Certificate Number: 40047657" respectively in Regulatory Information table. 11
- Changed CSA standard reference From:"Approved under CSA Component Acceptance Notice" To:"Approved according to IEC 60950-1 and IEC 61010-1" and document reference From: "File Number: pending" To:"Master Contract Number: 220991" respectively in Regulatory Information table. 11
- Changed UL standard reference From:"1577" To:"UL 1577" in Regulatory Information table. 11
- Changed ground symbol of 'Output' to differentiate it from 'Input' in Figure 6 12

Changes from Revision A (March 2012) to Revision B **Page**

- Changed signaling rate info from 1 to 50 Mbps. 1
- Changed Signaling rate max value from 1 to 50 Mbps, centered 0 in the min column. 4
- Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, changed 8.5 max value to 9.1. 5
- Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, changed 8.5 max value to 9.1 and changed 5.5 max value to 5.8. 6
- Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, changed 5.5 max value to 5.8 and changed 8.5 max value to 9.1. 7
- Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, changed 5.5 max

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7421EQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7421EQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISO7421E-Q1 :

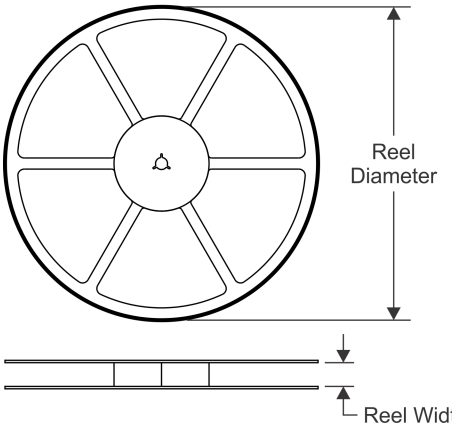
- Catalog: ISO7421E

NOTE: Qualified Version Definitions:

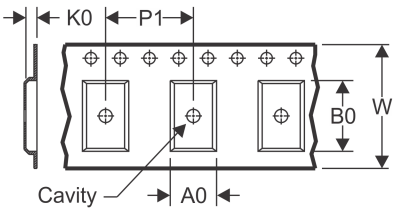
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

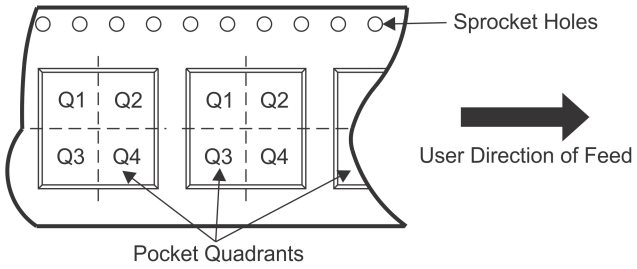


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

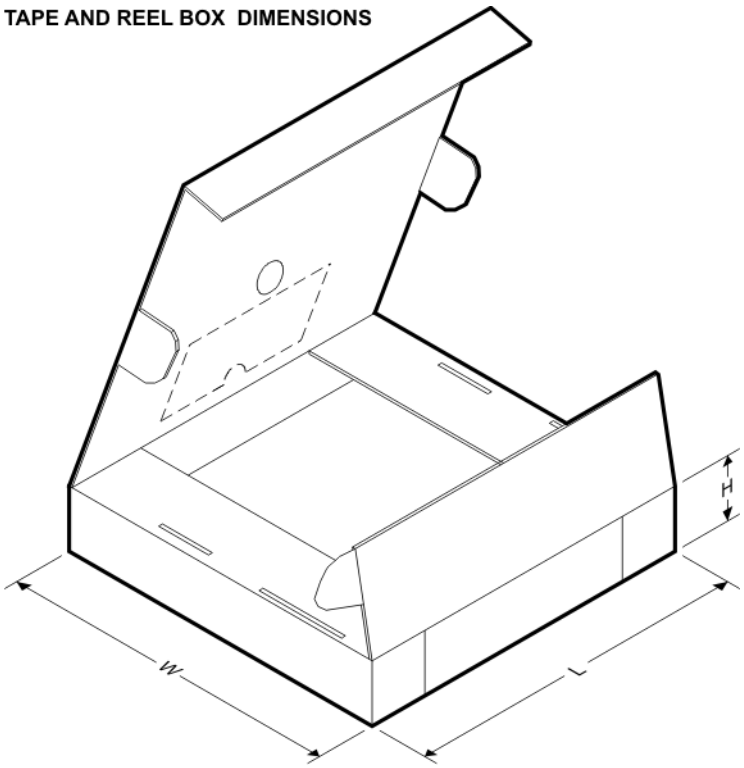
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7421EQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7421EQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

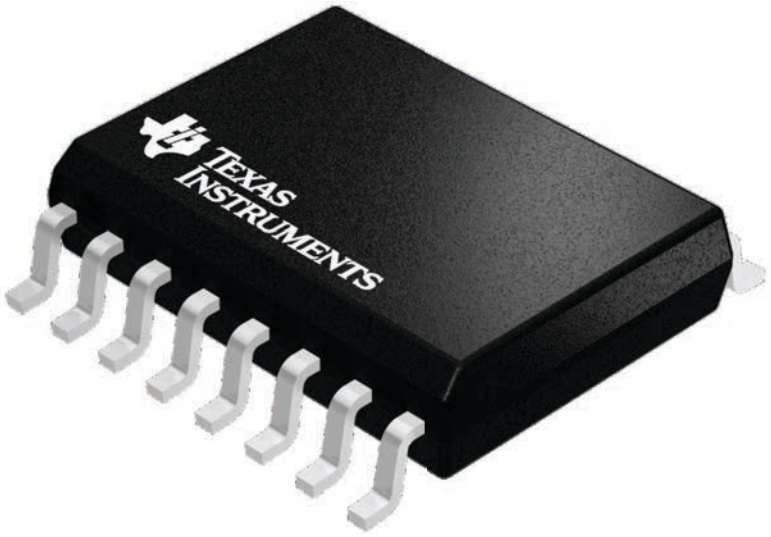
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

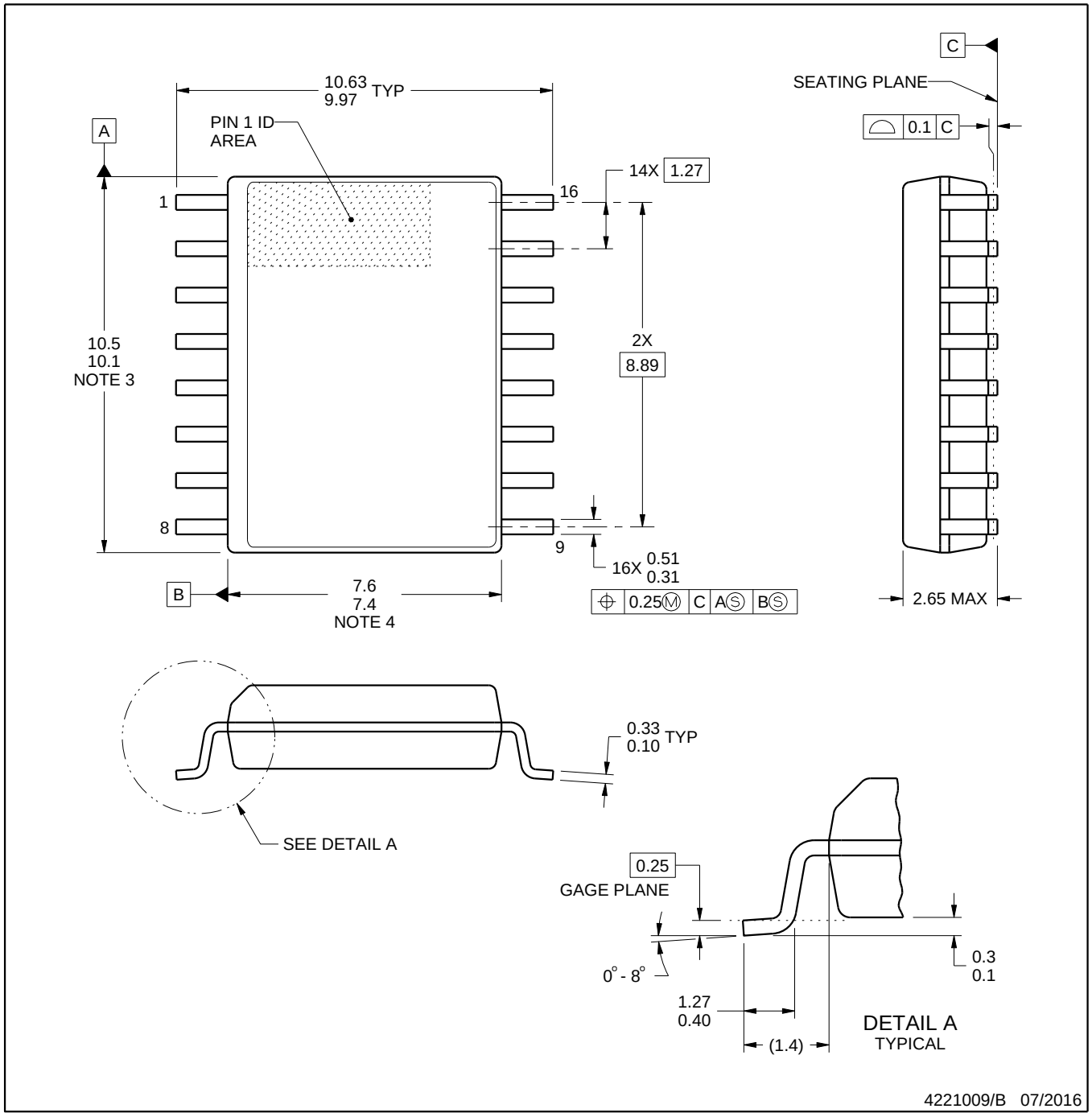
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



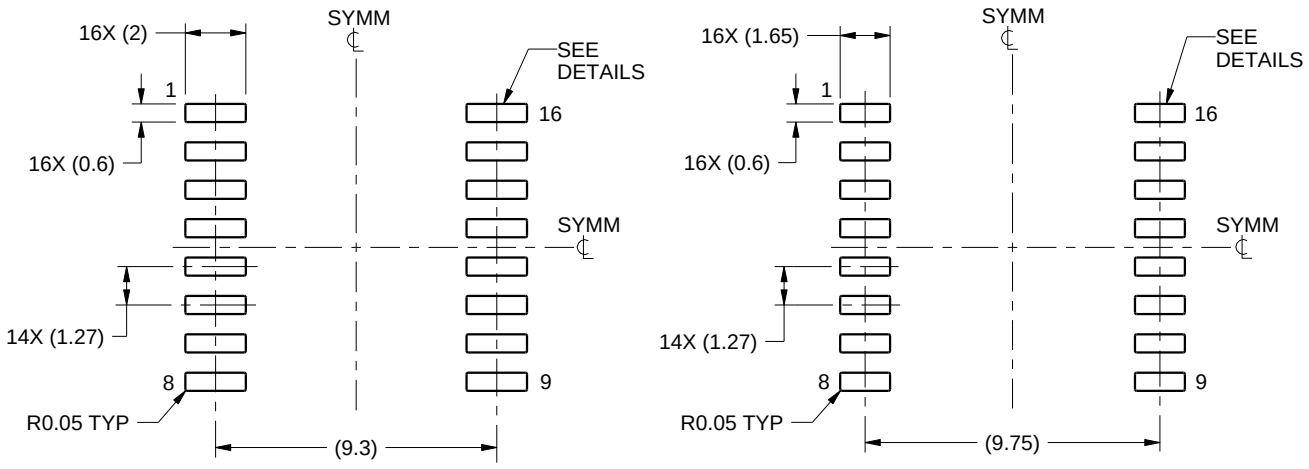
4224780/A

SOIC



NOTES:

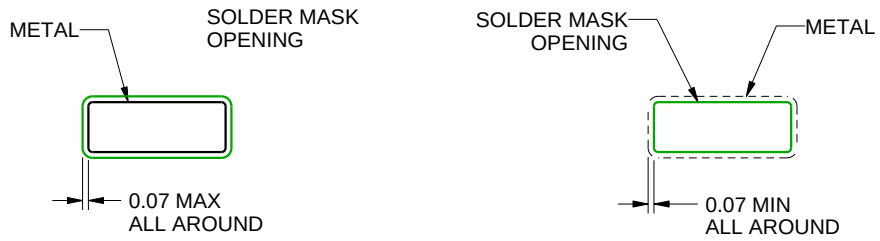
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

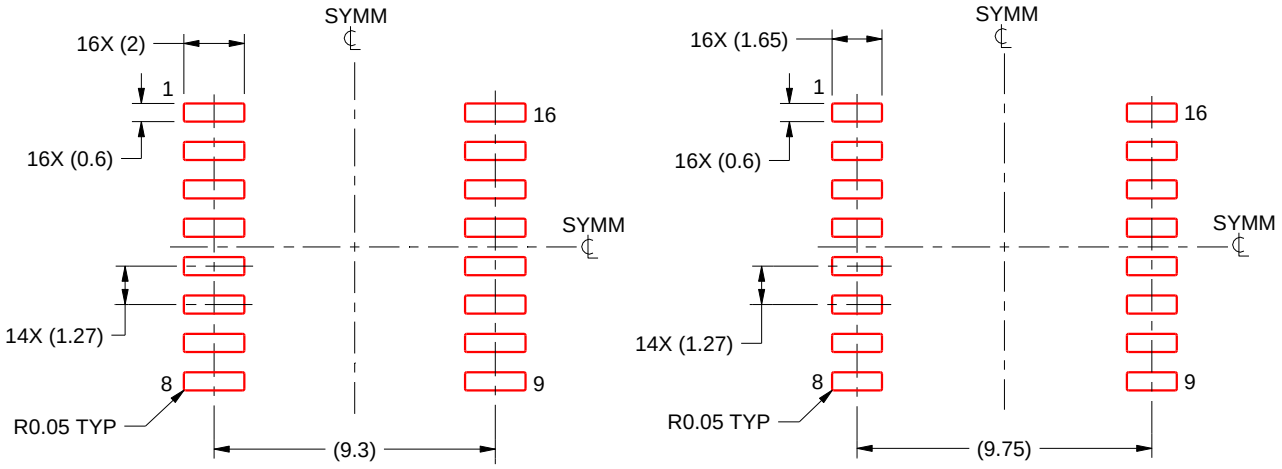
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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