CMT8603X Single-Channel Isolated Gate Driver

Features

- Safety-related certifications
  - DIN VDE V 0884-11: 2017-01
  - UL recognition: up to 5700 Vrms for 1 minute in SOW6; up to 5000 Vrms for 1 minute in DUB8
  - CSA component notice 5A
  - CQC approval per GB4943.1-2011
- Isolated single-channel driver
- Driver side supply voltage: up to 32V with UVLO
- Pin compatible, drop in upgrade for opto isolated gate drivers
- 4A peak source and 6A sink output current
- High CMTI: ±150 Kv/us
- 75ns typical propagation delay
- 30ns maximum pulse width distortion
- Operation temperature: - 40°C to 125°C
- Lead-free component, suitable for lead-free soldering profile: 260°C, MSL3
- RoHS & REACH Qualified: SOW6, SOP8 and DUB8

Applications

- DC to AC solar inverters
- Motor drivers
- UPS and battery charges
- Isolated DC/DC and AC/DC power supplies

Description

The CMT8603X is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. It can source 4A and 6A sink peak current. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 32V. While the input circuit imitates the characters of LEDs, it has performance advantages compared to standard opto-isolated gate drivers including better reliability and aging performance, higher working temperature, shorter propagation delay and smaller pulse width distortion.

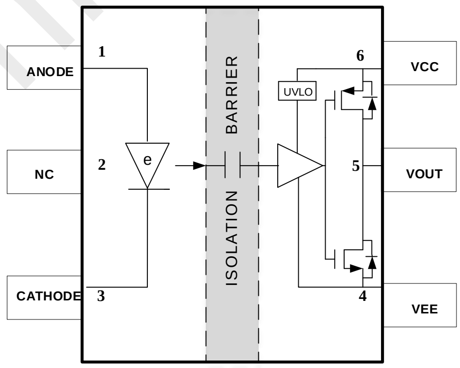
As a result, the CMT8603X is suitable to replace opto-isolated driver in high reliability, power density and efficiency switching power system.

The CMT8603X is available in SOW6 / SOP8 and DUB8 packages.

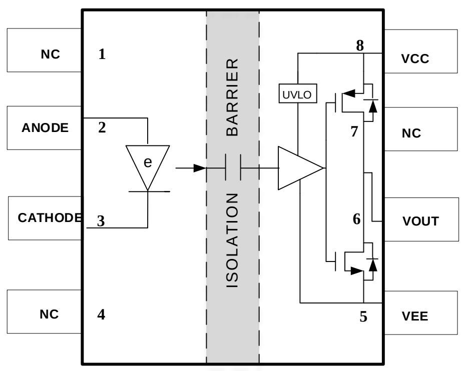
Device Information

Part No.	Package	Body Size (mm x mm)
CMT8603X-WF	SOW6	7.5mm * 4.68mm
CMT8603X-U	DUB8	9.32mm * 6.4mm
CMT8603X-N	SOP8	5.0mm * 3.90mm
Refer to section 9 for ordering information.		

Functional Block Diagram



CMT8603X SOW6 Block Diagram



CMT8603X DUB8/SOP8 Block Diagram

Table of Contents

1 Absolute Maximum Ratings

Table 1-1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Average Input Current	I_{F_AVG}		25	mA
Peak Transient Input Current	I_{F_PEAK}		0.2	A
Reverse Input Voltage	V_{R_MAX}		6.5	V
Driver Side Supply Voltage	V_{CC} - V_{EE}	- 0.3	35	V
Output Signal Voltage	V_{OUT}	V_{EE} - 0.3	V_{CC} + 0.3	V
Operating Junction Temperature	T_J	- 40	150	°C
Storage Temperature	T_{stg}	- 65	150	°C

2 Pin Description

The pin list is shown as below.

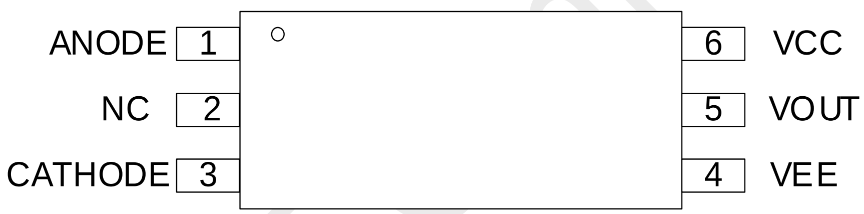


Figure 2-1. CMT8603X SOW6 Top View

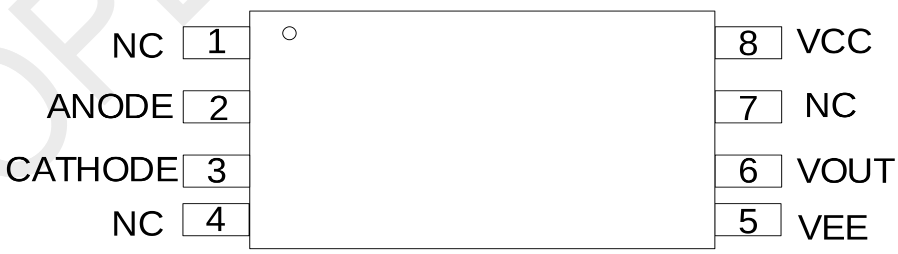


Figure 2-2. CMT8603X DUB8/SOP8 Top View

Table 2-1. Pin Description

Symbol	Pin No.		Description
	CMT8603X SOW6	CMT8603X DUB8/SOP8	
ANODE	1	2	Anode of LED emulator
CATHODE	3	3	Cathode of LED emulator
VCC	4	8	Positive output supply rail
VOUT	5	6	Gate-drive output
VEE	6	5	Negative output supply rail
NC	2	1,4,7	No Connection

3 Typical Application

3.1 Typical Application Schematic

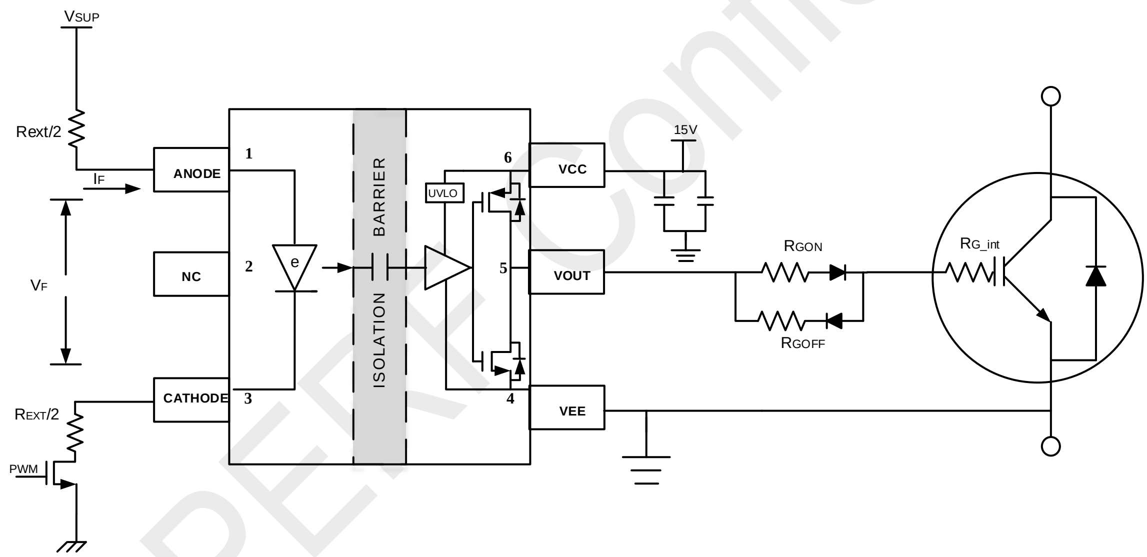


Figure 3-1. Typical Application Circuit with NMOS Driving Input Stage

Bypassing capacitors connecting between V_{CC} and V_{EE} are needed to achieve reliable performance. To filter noise, 0.1µF/50V ceramic capacitor is recommended to place as close as possible to CMT8603X. To support high peak currents when turning on external power transistor, additional 10µF/50V ceramic capacitor is recommended. If the V_{CC} power supply is located long distance from the IC, bigger capacitance is needed.

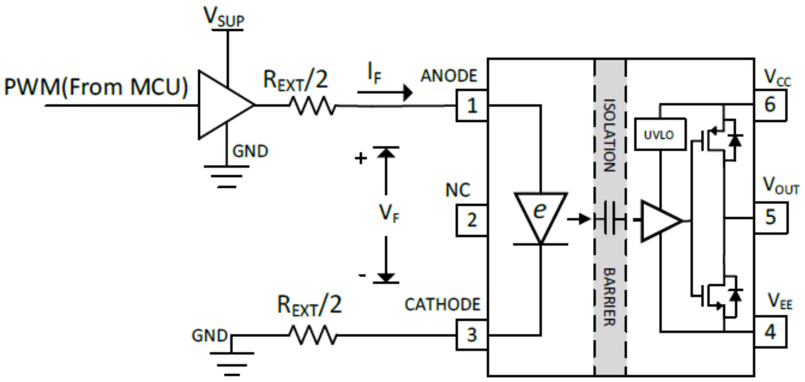


Figure 3-2. Typical Application Circuit with One Buffer Driving Input Stage

CMT8603X requires 7mA to 16mA bias current that flows into the e-diode for normal operation. The PWM from MCU is not suitable to provide such current directly and external circuit is needed. In Figure 3-1, one NMOS is used with split input resistors. Another input drive method is using one buffer, as shown in Figure 3-2.

3.2 Interlock Protection

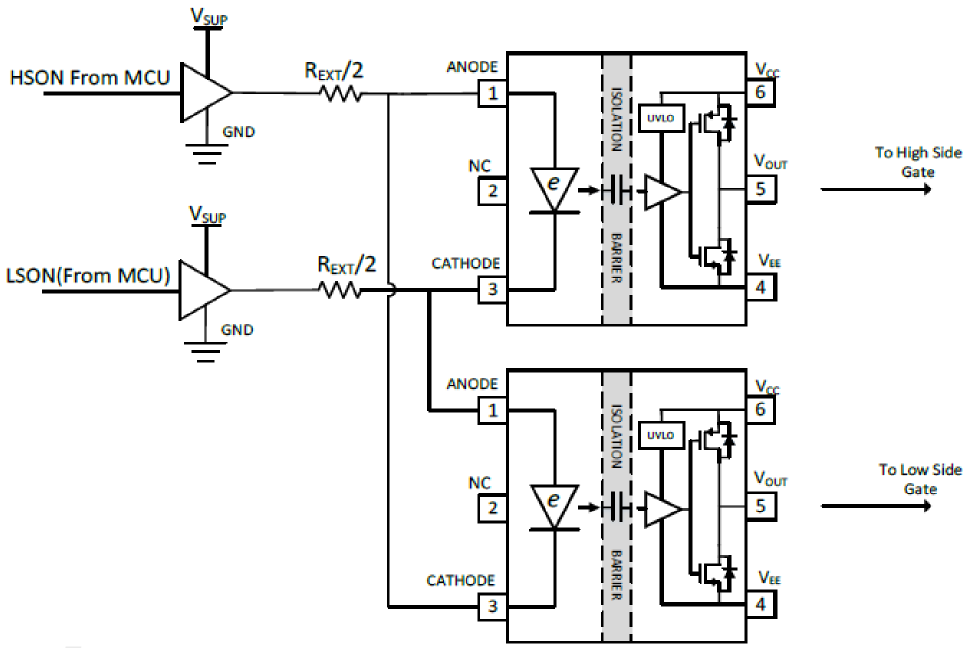


Figure 3-3. Interlock Protection using CMT8603X

For applications to drive power transistors in half bridge configuration, two CMT8603X can be used. Interlock protection is possible as shown in Figure 3-3. If the controller has some mistake, leading to negative dead time, the output PWM of CMT8603X is adjusted to avoid power transistor shoot through. The input side reverse breakdown voltage of CMT8603X is greater than 6.5V, which supports interlock protection of 3.3V or 5V PWM signal source.

3.3 Selecting Input Resistor

The recommended forward current range for CMT8603X is 7mA to 16mA. The value of input resistor, buffer supply voltage and buffer internal resistance influence the forward current, as shown in Equation (1). In Figure 3-1, R_{Buffer} is the on-resistance of the external NMOS. In Figure 3-2, R_{Buffer} is the buffer output impedance in output "High" state. In Figure 3-3, R_{Buffer} is the summary of buffer output impedance in "High" and "Low" state.

$$R_{EXT} = (V_{SUP} - V_F)/I_F - R_{Buffer} \quad (1)$$

The parameter variation needs to be taken into consideration when selecting input resistor.

Table 3-1. External Parameters Range when Calculating Input Resistor

Parameters	Min	Typ	Max	Unit
CMT8603X forward current I_F	7	10	16	mA
CMT8603X forward voltage V_F	1.8	2.1	2.4	V
Buffer supply voltage V_{SUP}	5*95%	5	5*105%	V
Buffer internal resistance R_{buffer}	13	18	22	Ω
External resistance R_{buffer}	203	272	314	Ω

3.4 PCB Layout Guidelines

Carful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to CMT8603X, between VCC to VEE.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place CMT8603X close to power transistor.
- Place large amount of copper connecting to VEE pin and VCC pin for thermal dissipation, with priority on VEE pin. If the system has multiple VEE or VCC layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

4 Parameter Measurement Circuit Setup

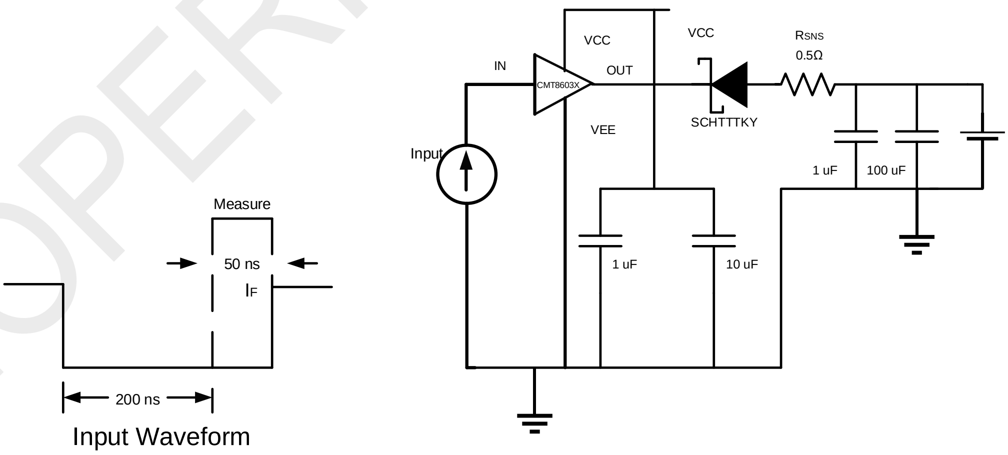


Figure 4-1. I_{OL} Sink Current Test Circuit

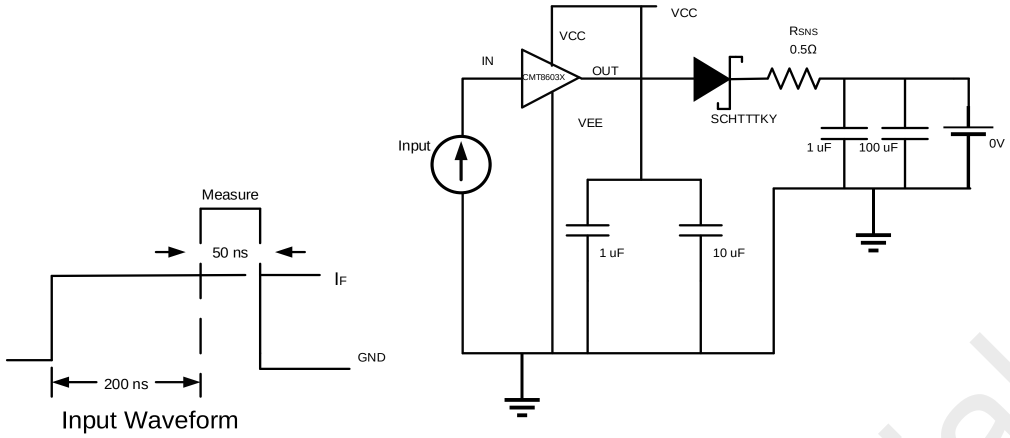


Figure 4-2. I_{OH} Source Current Test Circuit

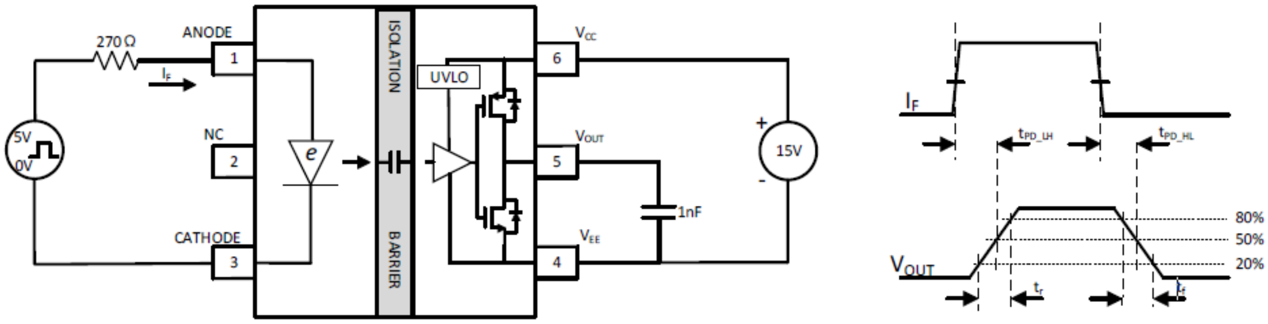


Figure 4-3. I_F to V_{OUT} Propagation Delay, Rise Time and Fall Time

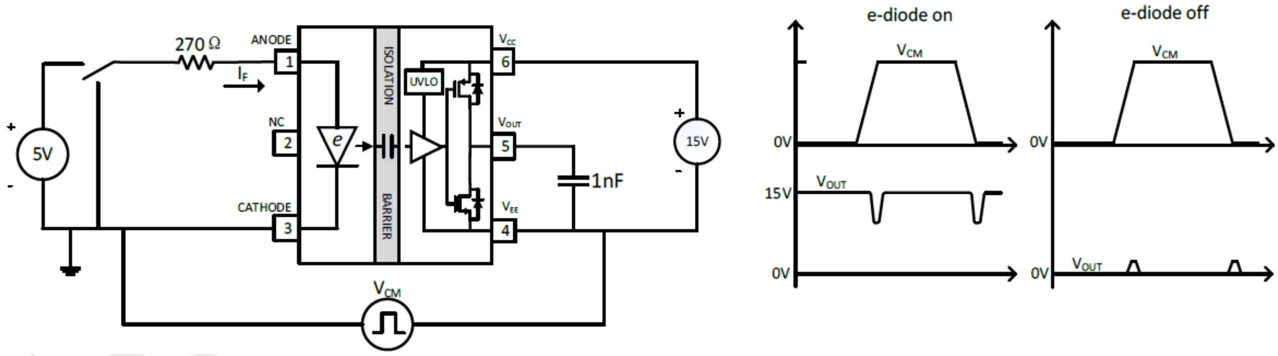


Figure 4-4. Common Mode Transient Immunity Test Circuit

5 Specifications

5.1 DC Electrical Characteristics

All min and max specifications are at T_J = -40°C to 150°C, V_{CC} = 14V - 32V, V_{EE} = GND, $I_{F(ON)}$ = 7mA - 16mA, $V_{F(off)}$ = -5.5V - 0.9V). Unless otherwise noted, typical values are at V_{CC} = 15V, V_{EE} = GND, T_A = 25 ℃.

Table 5-1. Electrical Characteristics

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Driver Side Supply						
High level supply current	I_{CCH}	I_F = 10mA, I_{OUT} = 0mA		1.7	3	mA
Low level supply current	I_{CCL}	V_F = 0V, I_{OUT} = 0mA		1.6	3	mA
Driver Side Supply UVLO Threshold (CMT8603X, 13V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC_ON}	I_F = 10mA	12.6	13.2	13.7	V
VCC UVLO Falling Threshold	V_{CC_OFF}		11.7	12.3	12.7	
VCC UVLO Hysteresis	V_{CC_HYS}			0.9		
Driver Side Supply UVLO Threshold ((CMT8603X, 9V UVLO Level)						
VCC2 UVLO Rising Threshold	V_{CC2_ON}	I_F = 10mA	8.7	9.2	9.7	mV
VCC2 UVLO Falling Threshold	V_{CC2_OFF}		8	8.5	9	
VCC2 UVLO Hysteresis	V_{CC2_HYS}			0.7		
Input Pin Characteristic						
Input Forward Threshold Current Low to High	I_{FLH}	VOUT > 5V, Cg = 1nF	1.5	2.7	4	mA
Threshold Input Voltage High to Low	V_{FHL}	VOUT < 5V, Cg = 1nF	0.9			V
Input Forward Voltage	V_F	I_F = 10mA	1.8	2.1	2.4	V
Temp Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T$	I_F = 10mA		0.34		mV/℃
Input Reverse Breakdown Voltage	V_R	I_R = 10uA	6.5			V
Input Capacitance	C_{IN}	f = 1MHz		17		pF
Output Pin Characteristic						
High Level Output Voltage	V_{OH}	I_{OUT} = -50mA, I_F = 10mA	V_{CC} - 0.3	V_{CC} - 0.15		V
		I_{OUT} = 0mA, I_F = 10mA		V_{CC}		
Low Level Output Voltage	V_{OL}	I_{OUT} = 50 mA, V_F = 0 V		30	65	mV
High Level Peak Output Current	I_{OH}	V_{CC} = 15V, pulse width < 10us		4		A
Low Level Peak Output Current	I_{OL}	V_{CC} = 15V, pulse width < 10us		6		

5.2 Switching Electrical Characteristics

All min and max specifications are at T_J = -40° C to 150° C, V_{CC} = 14V - 32V, V_{EE} = GND, $I_{F(ON)}$ = 7mA - 16mA, $V_{F(off)}$ = -5.5V - 0.9V) . Unless otherwise noted, typical values are at V_{CC} = 15V, V_{EE} = GND, TA = 25 ℃.

Table 5-2. Switching Electrical Characteristics

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay	t_{PLH}	C_{LOAD} = 1nF, f = 20kHz (50% Duty Cycle)	50	75	100	ns
	t_{PHL}		50	69	100	ns
Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	t_{PWD}			6	30	ns
Propagation Delay Difference Between Any Two Parts ($t_{PHL} - t_{PLH}$) (1)	PDD		-35		35	ns

Output Rise Time (20% to 80%)	t_R			6	20	ns
Output Fall Time (80% to 20%)	t_F			6	20	ns
Common Mode Transient Immunity	CMTI		150			kV/us
(1) The difference between t_{PHL} and t_{PLH} between any two parts under the same test condition, ensured by characterization.						

5.3 Insulation Specifications

Table 5-3. Insulation Specifications

Parameters	Sym.	Condition	Value			Unit
			SOW6	DUB8	SOP8	
External clearance	CLR	The shortest terminal-to-terminal distance through air	8.0	6.5	4.0	mm
External creepage	CRP	The shortest terminal-to-terminal distance across the package surface	8.0	6.5	4.0	mm
Distance through insulation	DTI	Minimum internal gap	>30			um
Comparative tracking index	CTI	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	> 600	> 400	V
Material group	-	IEC 60664-1	I	I	I	-

5.4 Insulation Characteristics for SOW6 / DUB8 / SOP8 Package

Description	Test Condition	Symbol	Value			Unit
			SOW6	DUB8	SOP8	
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ $600V_{RMS}$		I to IV			
	For Rated Mains Voltage ≤ $1000V_{RMS}$		I to III			
Climatic Category			40/125/21			
Pollution Degree	per DIN VDE 0110		2			
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	1000	400	V_{RMS}
	DC voltage		2121	1414	565	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	2121	1414	565	V_{PEAK}
Apparent Charge	Method B, routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2*V_{IOTM}$, $V_{pd(m)} = V_{IORM}×1.875$, $t_{ini} = t_m = 1s$	q_{pd}	<5			pC
	Method A, after Environmental Tests Subgroup 1, $V_{pd(m)} = V_{IORM}×1.6$, $t_{ini} = 60s$, $t_m = 10s$					
	Method A, after Input and Output Safety Test Subgroup 2 and Subgroup 3, $V_{pd(m)} = V_{IORM}×1.2$, $t_{ini} = 60s$, $t_m = 10s$					

Maximum Transient Isolation Voltage	t = 60s	V_{IOTM}	8000	7000	5300	V_{peak}
Maximum Withstanding Isolation Voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	V_{ISO}	5700	5000	3750	V_{RMS}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = V_{IOSM} \times 1.6$	V_{IOSM}	8000	7000	5300	V_{peak}
Isolation Resistance	V_{IO} = 500V at $T_A = T_S$= 25°C	R_{IO}	$>10^{12}$			Ω
	V_{IO} = 500V at $T_A = T_S$= 150°C		$>10^{9}$			
	V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C		$>10^{11}$			
Isolation Capacitance	f = 1MHz	C_{IO}	1			pF

5.5 Safety-Limiting Values for SOW6 / DUB8 Package

Description	Test Condition	Symbol	Value	Unit
Maximum Safety Temperature		T_S	150	℃
Safety Input, Output, or Total Power	$R_{\theta JA}$ = 125°C/W, T_J = 150°C, T_A = 25°C	P_S	750	mW
Safety Input, Output, or Supply Current	$R_{\theta JA}$ = 125°C/W, T_J = 150°C, T_A = 25°C	I_S	50	mA
	$R_{\theta JA}$ = 125°C/W, V_{CC} = 30V, T_J = 150°C, T_A = 25°C		25	

5.6 Safety-Limiting Values for SOP8 Package

Description	Test Condition	Symbol	Value		Unit
Maximum Safety Temperature		T_S	150		℃
Safety Input, Output, or Total Power	$R_{\theta JA}$ = 110°C/W, T_J = 150°C, T_A = 25°C	P_S	Total	1.14	W
			Input side	0.05	
			Output side	1.09	
Safety Input, Output, or Supply Current	$R_{\theta JA}$ = 110°C/W, V_{CC} = 15V T_J = 150°C, T_A = 25°C	I_S	50		mA
	$R_{\theta JA}$ = 110°C/W, V_{CC} = 30V, T_J = 150°C, T_A = 25°C		25		

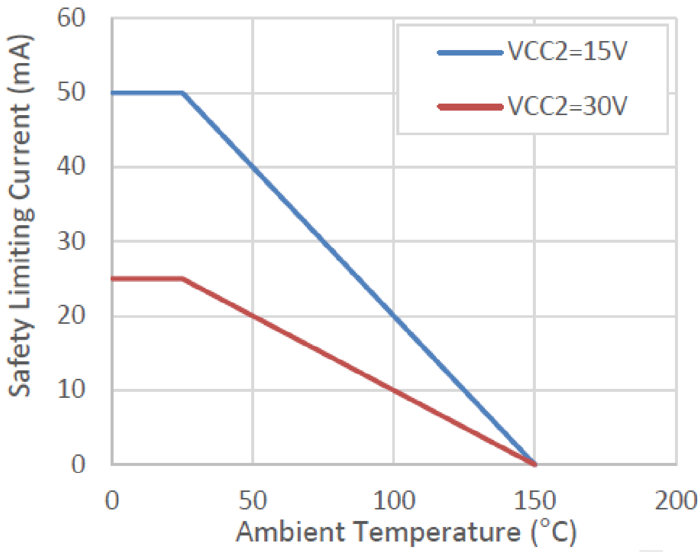


Figure 5-1. Thermal Derating Curve for Limiting Current per DIN VDE V 0884-11

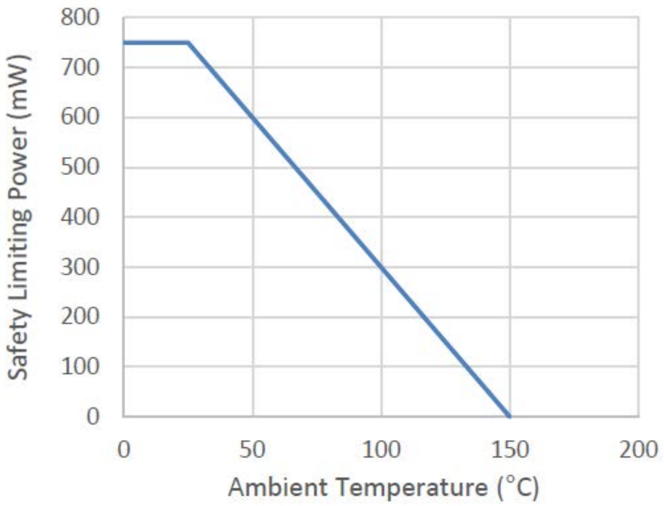


Figure 5-2. Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11

5.7 Typical Performance

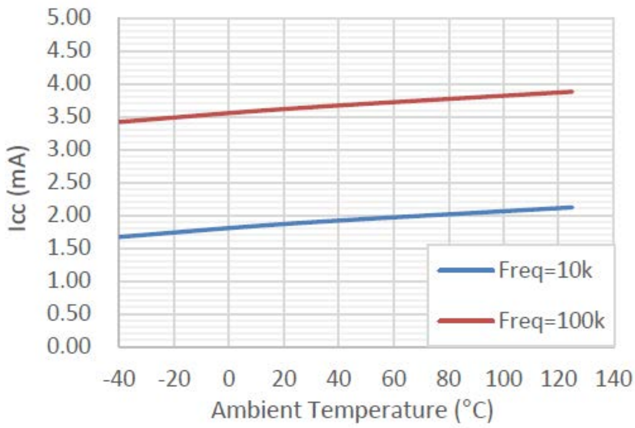


Figure 5-3. Supply Current vs Temperature

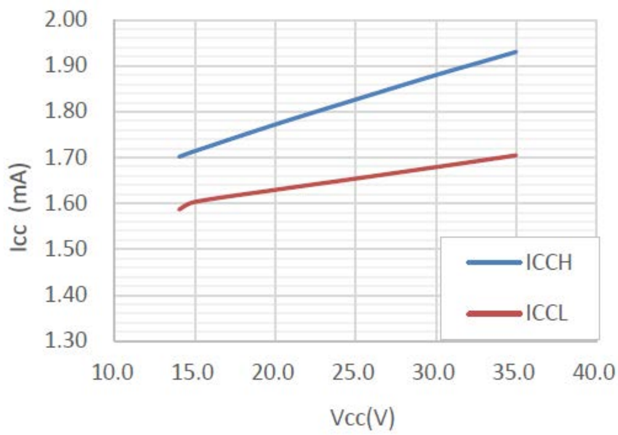


Figure 5-4. Supply Current vs Supply Voltage

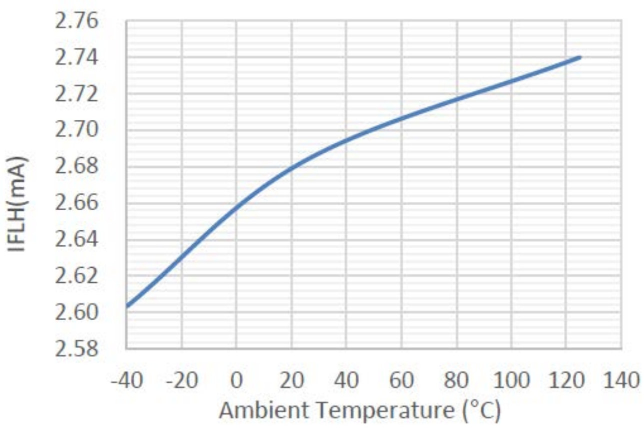


Figure 5-5. Forward Threshold Current vs Temperature

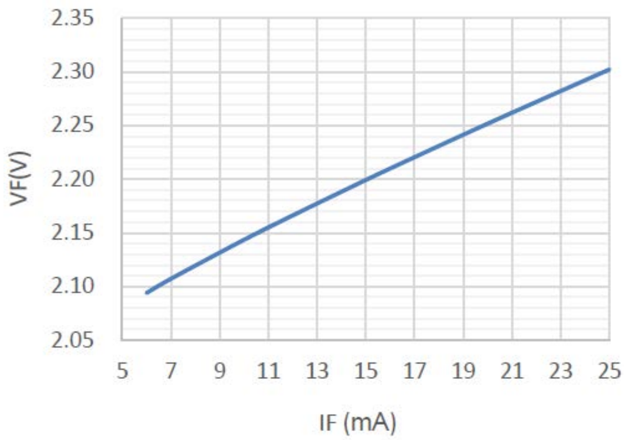


Figure 5-6. Forward Current vs Forward Voltage Drop

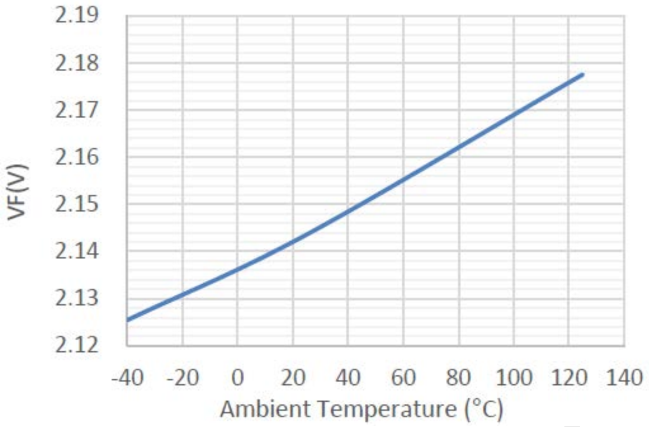


Figure 5-7. Forward Voltage Drop vs Temperature

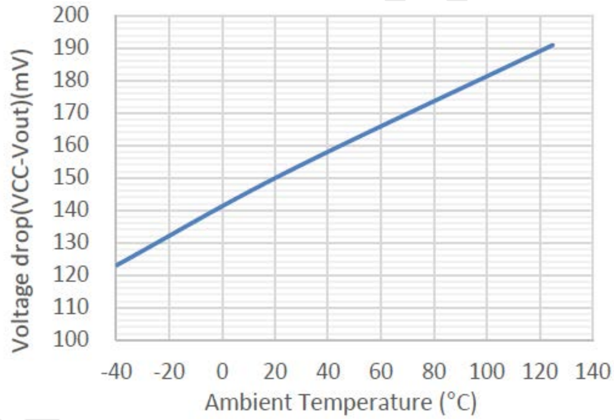


Figure 5-8. V_{OH} (50mA Load) vs Temperature

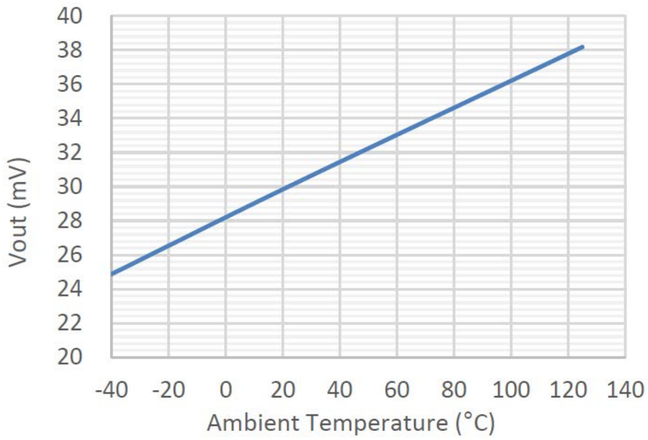


Figure 5-9. V_{OL} vs Temperature

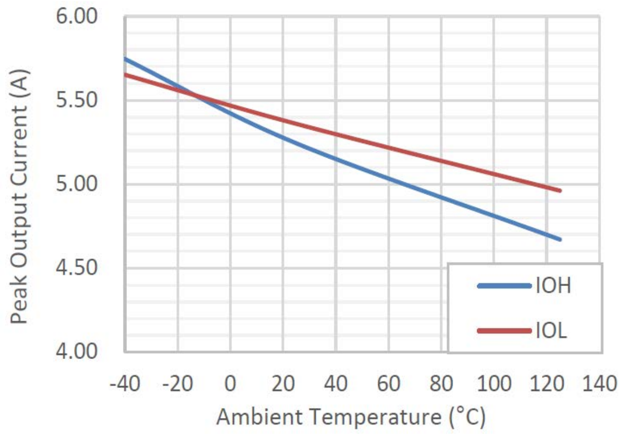


Figure 5-10. Output Drive Currents vs Temperature

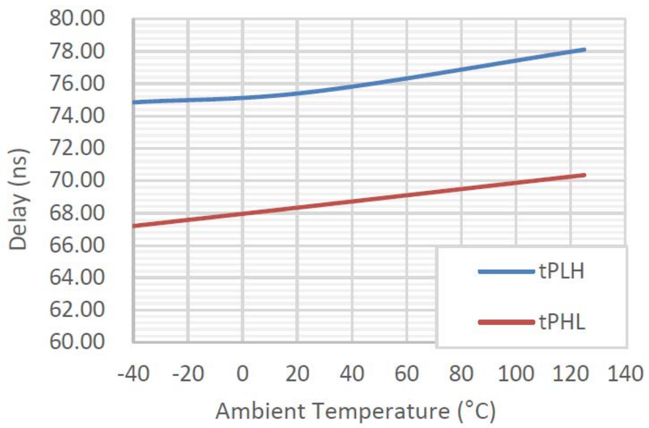


Figure 5-11. Propagation Delay vs Temperature

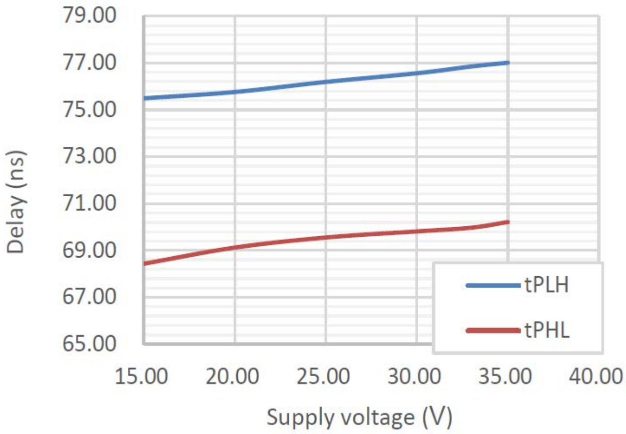


Figure 5-12. Propagation Delay vs Supply Voltage

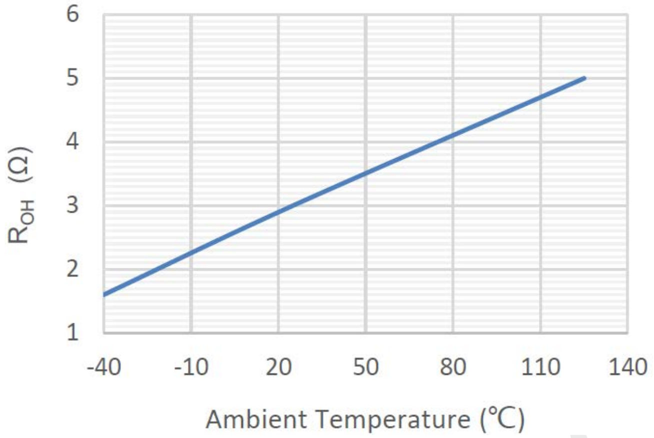


Figure 5-13. R_{OH} vs Temperature

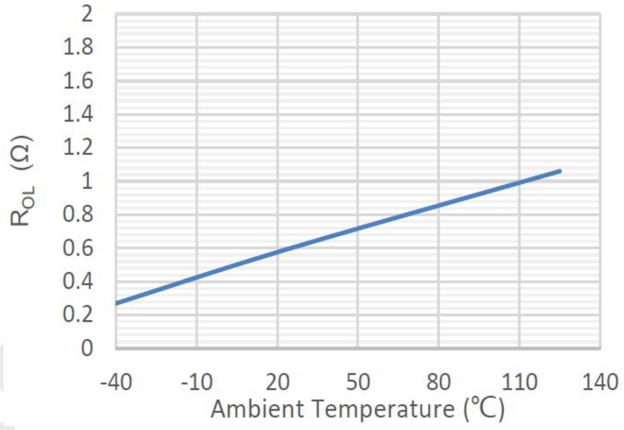


Figure 5-14. R_{OL} vs Supply Voltage

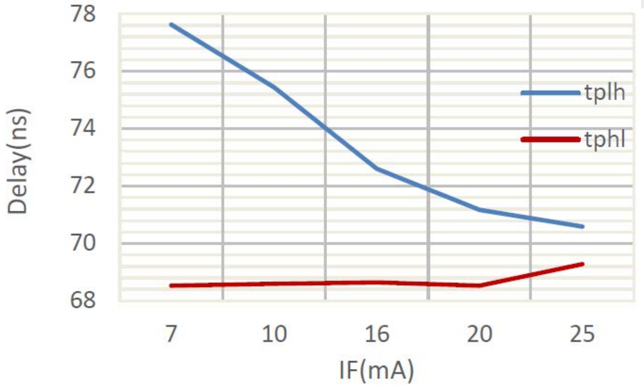


Figure 5-15. Propagation Delay vs Forward Current

6 Safety-related Certifications

6.1 Regulatory Information

UL	CSA	VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN EN IEC 60747-17(VDE 0884-17)	Certified by CQC11-471543-2012GB4943.1-2022
Pending		Pending	Pending

7 Function Description

7.1 Function Overview

The CMT8603X is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. The integrated galvanic isolation between control input logic and driving output stage grants additional safety. The device can source 4A and sink 6A peak current, which can drive IGBTs, power MOSFETs and SiC MOSFETs in many applications such as motor control systems, solar inverters and power supplies.

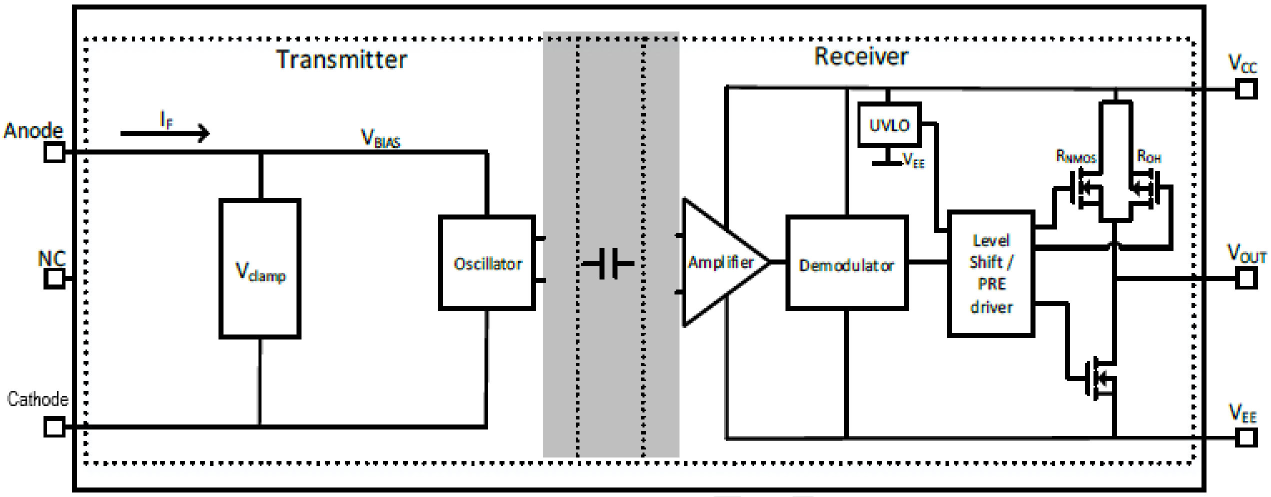


Figure 7-1. CMT8603X Functional Block Diagram

7.2 Truth Tables

Table 7-1. Driver Function Table[1]

e-diode	V_{CC} status	Outputs
X	Powered down	L
$I_F > I_{FLH}$	Powered up	H
$V_F > V_{FLH}$	Powered up	L

1) H= Logic High; L= Logic Low; X= Irrelevant

7.3 Output Stage

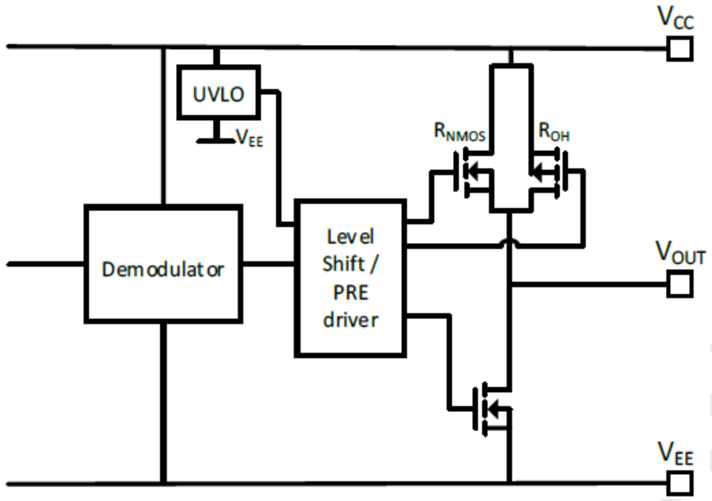


Figure 7-2. CMT8603X Output Stage

Table 7-2. CMT8603X Output Stage On-Resistance

R_{NMOS}	R_{OH}	R_{OL}	Unit
1.4	5	0.6	Ω

The CMT8603X has P-channel and N-channel MOSFET in parallel to pull up the OUT pin when turning on external power transistor. During DC measurement, only the P-channel MOSFET is conducting. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET.

The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the CMT8603X N-channel MOSFET turns on to pull up OUT more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to smaller temperature increase of CMT8603X. The equivalent pull-up resistance of CMT8603X is the parallel combination R_{OH} || R_{NMOS}. The result is quite small, indicating the strong driving capability of CMT8603X.

The pull-down structure of CMT8603X is simply composed of an N-channel MOSFET with on-resistance of R_{OL}. The result is quite small, indicating the strong driving capability of CMT8603X.

7.4 VCC and Under Voltage Lock Out (UVLO)

The lower limit of driver side supply voltage (V_{CC}) is determined by the internal UVLO protection feature of the device. V_{CC} voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low.

A local bypass capacitor should be placed between the V_{CC} and V_{EE} pins, with a value of 220nF to 10μF for device biasing. An additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

7.5 Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC} is not connected to the power supply. When V_{CC}

is floating, the driver output is held low and clamping V_{OUT} pin to approximately 1.9V higher than V_{EE}.

7.6 Short Circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the Miller capacitance. The diode between V_{OUT} and V_{CC} pins inside the driver limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500mA may be fed back to the supply through this path for 10μs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

7.7 Thermal Shutdown

Parameter	Symbol	CMT8603X			Unit
		SOW6	DUB8	SOP8	
Junction–to-ambient thermal resistance	$R_{\theta JA}$	125	110	110	℃/W
Junction–to-top characterization parameter	Ψ_{JT}	30	30	18	℃/W

8 Packaging Information

The packaging information of the CMT8603X is shown in the figures below.

8.1 CMT8603X SOW6 Packaging

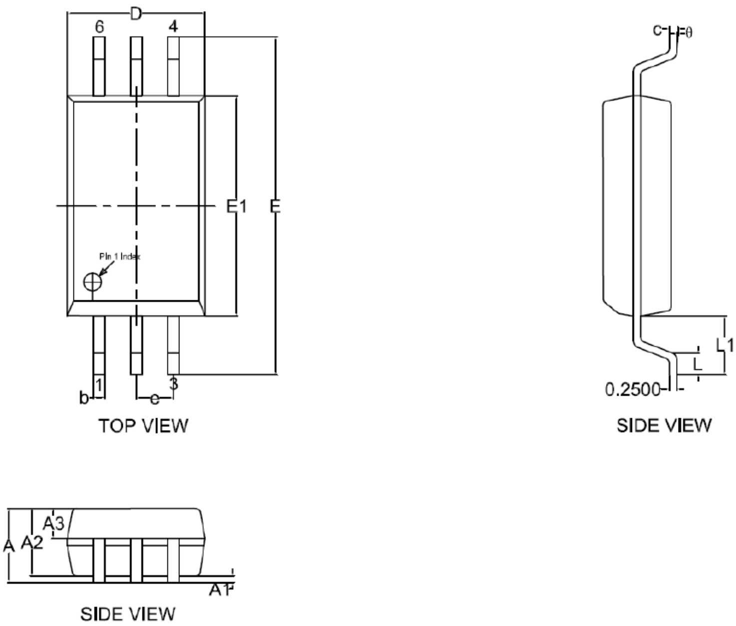


Figure 8-1. SOW6 Packaging

Table 8-1. SOW6 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
E	11.25	11.50	11.75
E1	7.40	7.50	7.60
D	4.58	4.68	4.78
L	0.50	-	1.00
b	0.28	-	0.51
c	0.25	-	0.29
θ	0°	-	8°
e	1.27 BSC		
L1	2.00 BSC		

8.2 CMT8603X DUB8 Packaging

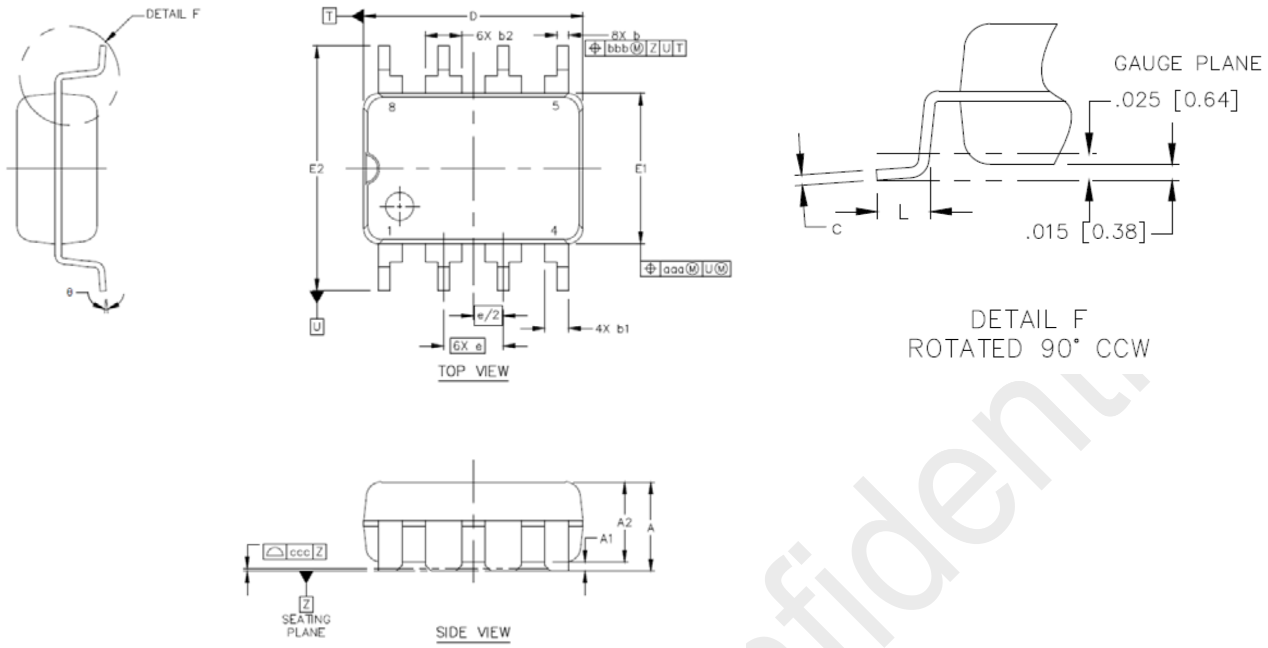
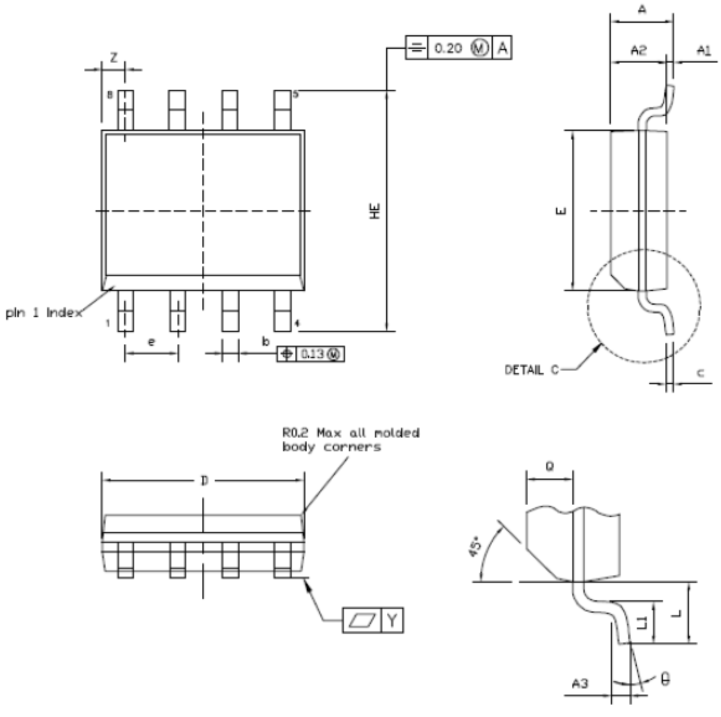


Figure 8-2. DUB Packaging

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	3.58	---	4.19
STAND OFF	A1	0.38	---	0.58
MOLD THICKNESS	A2	3.20	---	3.61
LEAD WIDTH	b	0.36	---	0.56
	b1	---	0.99 REF	---
	b2	---	1.524 REF	--
L/F THICKNESS	c	0.20	---	0.36
BODY SIZE	D	9.27	---	9.37
	E1	6.20	---	6.60
	E2	10.11	---	10.69
LEAD PITCH	e	2.54 BSC		
LEAD LENGTH	L	1.15	---	1.45
	θ	0°	---	8°
LEAD OFFSET	aaa	0.254		

Table 8-2. DUB8 Packaging Scale

8.3 CMT8603X SOP8 Packaging



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

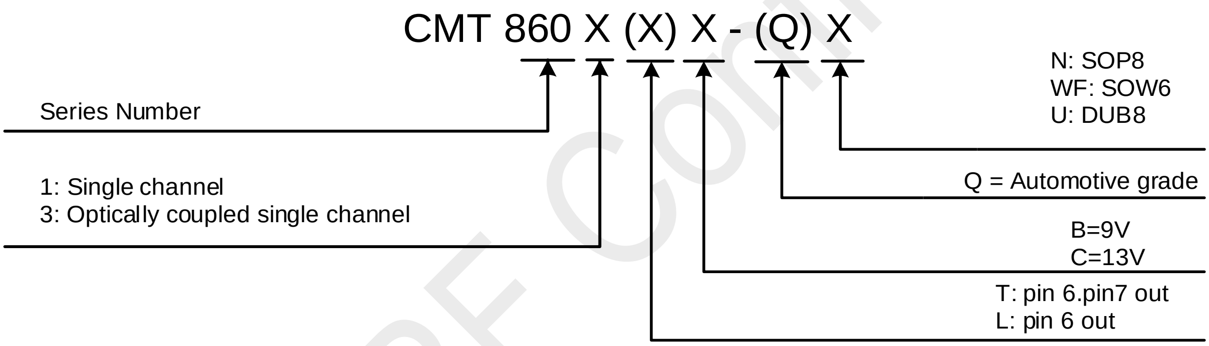
Figure 8-3. SOP8 Package Shape and Dimension in Millimeters

9 Ordering Information

Table 2. Part Number List

Part Number	MOQ	Isolation Rating (kV_{rms})	UVLO Level	Vout Connection	MSL	Temperature	Package
CMT8603B-N	3000	3.75	9	6	1	-40 to 125℃	SOP8
CMT8603B-WF	1000	5.7	9	5	3	-40 to 125℃	SOW6
CMT8603B-U	1000	5	9	6	3	-40 to 125℃	DUB8
CMT8603C-N	3000	3.75	13	6	1	-40 to 125℃	SOP8
CMT8603C-WF	1000	5.7	13	5	3	-40 to 125℃	SOW6
CMT8603C-U	1000	5	13	6	3	-40 to 125℃	DUB8

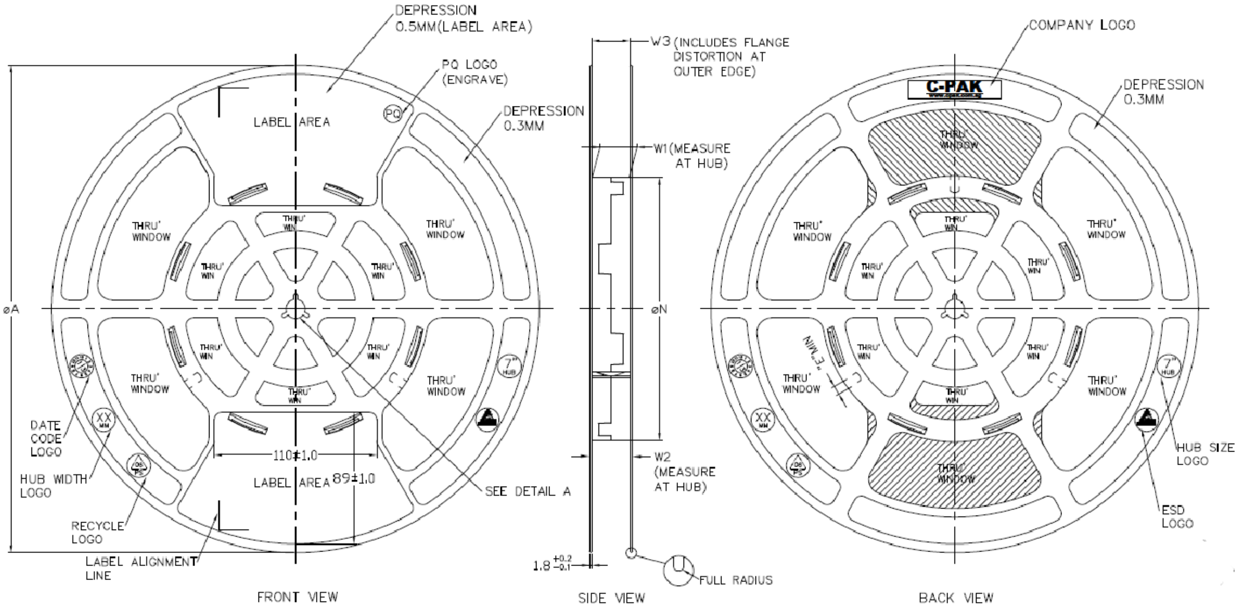
Part Number Naming Rule:

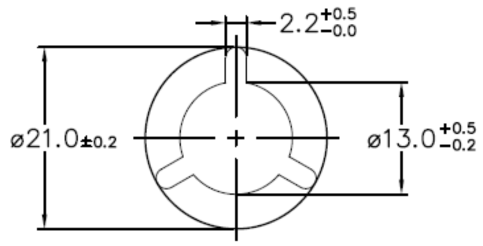


Please visit www.hoperf.com for more product/product line information.

Please contact sales@hoperf.com or your local sales representative for sales or pricing requirements.

10 Tape and Reel Information





ARBOR HOLE
DETAIL A
SCALE : 3:1

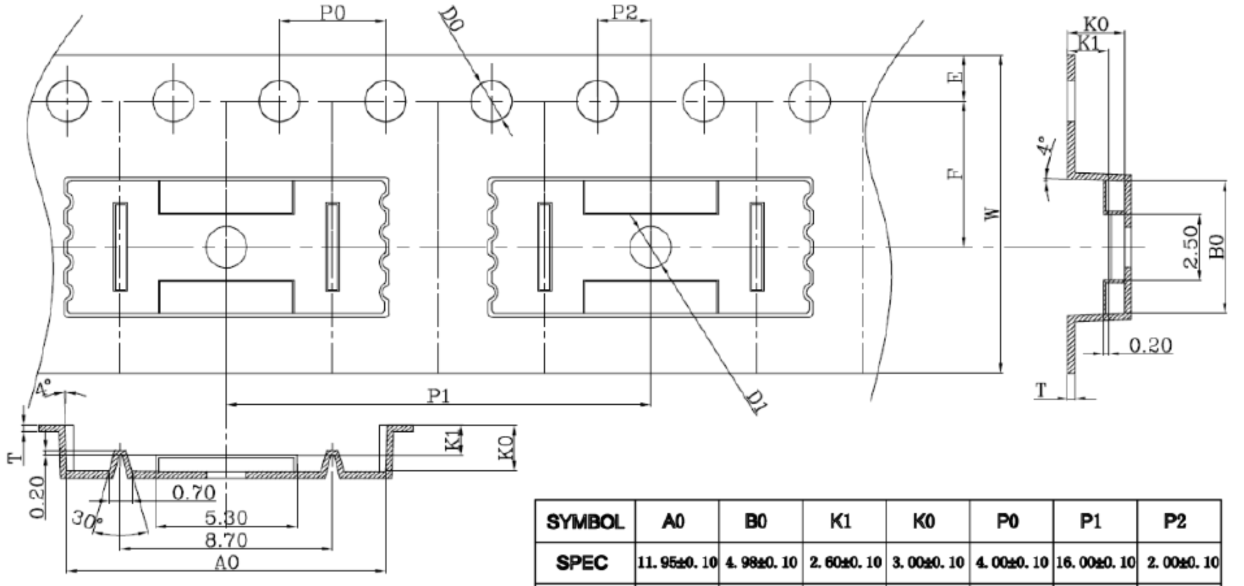
PRODUCT SPECIFICATION

TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY

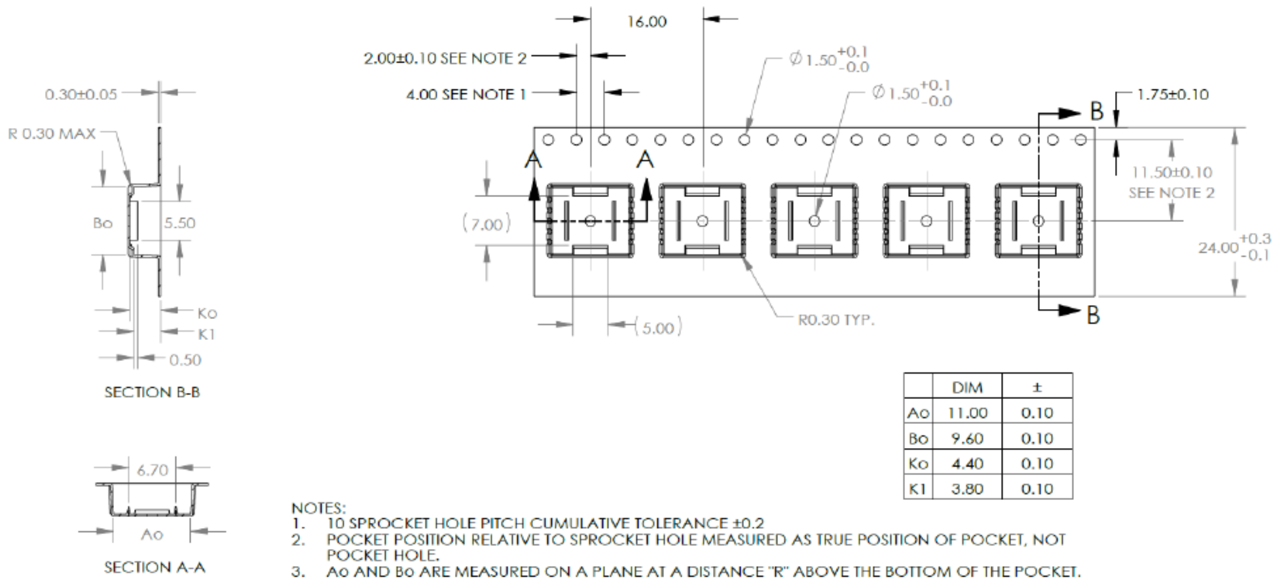
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 10-1. CMT8603X Tape and Reel Information



SYMBOL	A0	B0	K1	K0	P0	P1	P2
SPEC	11.95±0.10	4.98±0.10	2.60±0.10	3.00±0.10	4.00±0.10	16.00±0.10	2.00±0.10
SYMBOL	T	E	F	D0	D1	W	
SPEC	0.30±0.03	1.75±0.10	5.50±0.05	1.55±0.05	1.55±0.10	$12.0^{+0.30}_{-0.10}$	

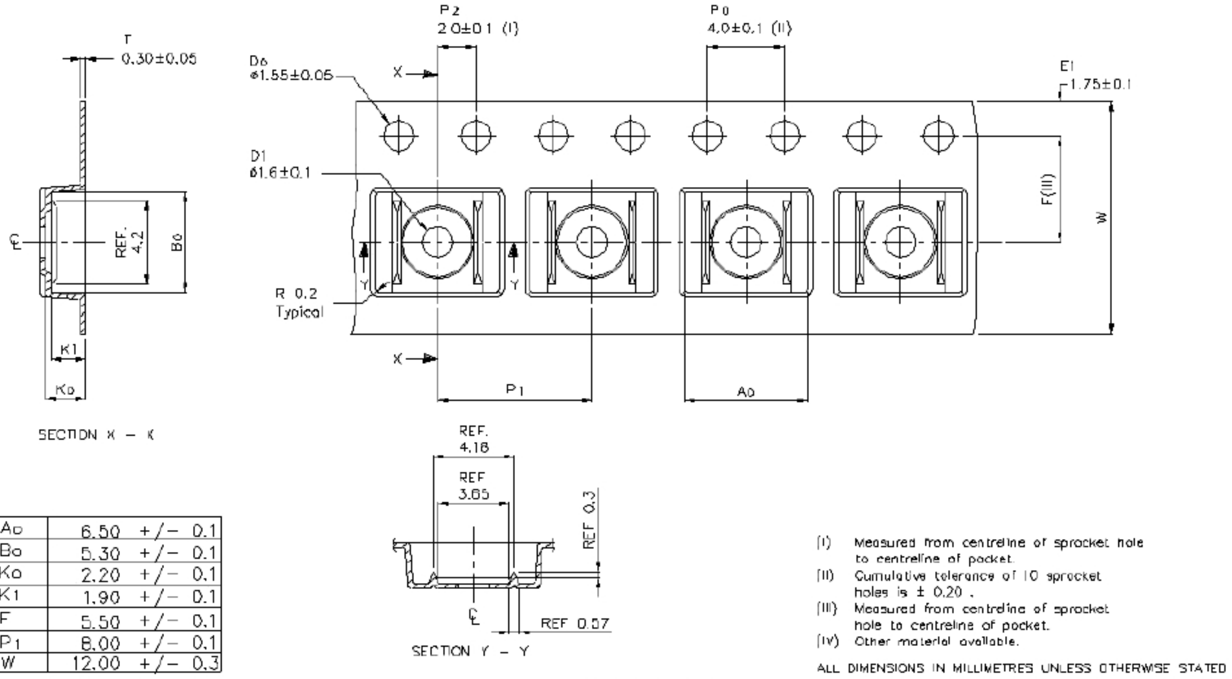
Figure 10-2. Tape Information of SOW6



	DIM	±
Ao	11.00	0.10
Bo	9.60	0.10
Ko	4.40	0.10
K1	3.80	0.10

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 10-3. Tape Information of DUB8



Ao	6.50 +/− 0.1
Bo	5.30 +/− 0.1
Ko	2.20 +/− 0.1
K1	1.90 +/− 0.1
F	5.50 +/− 0.1
P1	8.00 +/− 0.1
W	12.00 +/− 0.3

Figure 10-4. Tape Information of SOP8

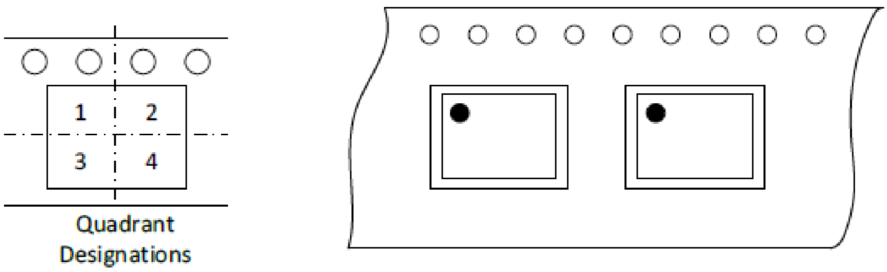


Figure 10-5. Quadrant Designation for Pin1 Orientation in Tape

11 Revise History

Table 3-1. Revise Records

Version No.	Chapter	Description	Date
0.1	All	Initial version	2024/03/29

12 Contacts

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